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Fabrication of high performance top-gate complementary inverter using a single carbon nanotube and via a simple process

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High performance complementary inverters have been fabricated using single-walled carbon nanotubes. The Al_2O_3 top-gate dielectric is grown via first depositing an Al film followed by complete oxidation of the film. It is shown that the quality of the Al_2O_3 film can be significantly improved by annealing at 400 °C, and stable *p*-type and *n*-type carbon nanotube field-effect transistors (CNTFETs) may be fabricated using either Pd (*p*-type) or Al (*n*-type) electrodes. High performance complementary inverter is demonstrated by integrating the *p*-type and *n*-type CNTFETs on the same carbon nanotube, and a gain of about 3.5 is achieved. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2745646]

Carbon nanotube (CNT) field-effect transistors (CNTFETs) have been fabricated and researched extensively because of their potential application in nanoelectronics.[1] While high performance *p*-type CNTFETs have been fabricated by many groups around the world,[2–4] only a few reported stable high performance *n*-type CNTFETs (Refs. 5–8) and even fewer reported on the fabrication of complementary inverters with a gain of more than 1.[9–12]

Early CNTFETs were fabricated mainly using the back-gate (or bottom gate) geometry and SiO_2 as the gate oxide. This CNTFET configuration is easy to fabricate and results in high I_{on}/I_{off} ratio (typically larger than 10^5).[13,14] However, the typical back-gate oxide thickness is a few hundred nanometers, which limits the performance of the CNTFETs and separate control on individual CNTFETs is difficult with this geometry. The introduction of high κ materials for gate oxide[2] and the top-gate geometry[3,11] has dramatically changed the situation for fabricating high performance CNTFETs. Various high κ materials have been attempted, including ZrO_2,[11] HfO_2,[8,15] Al_2O_3,[12] and TiO_2.[16] Usually high quality high-κ top-gate oxides were grown using atomic layer deposition technique. In this letter we report a simple procedure for fabricating both *p*- and *n*-type stable CNTFETs and high performance complementary inverter on a single CNT with Al_2O_3 top-gate oxides using electron beam evaporation technique, and show that the performance of the fabricated top-gate CNTFETs is much improved comparing with that of the SiO_2 back-gated CNTFETs. It has been shown that CNTFETs can outperform state-of-the-art silicon FETs in many ways[1–12] because of their near ballistic electrical transport and chemical robustness. CNT is intrinsically compatible with high-κ dielectrics due to the lack of dangling bonds at the nanotube/high-κ dielectric interface and the weak noncovalent bonding interactions between the two materials. As a result electron transport in CNT is hardly affected by the presence of high-κ dielectric, while it is not true in the case of silicon complementary metal-oxide semiconductor (CMOS).

Ultralong single-wall CNTs (SWCNTs) (Refs. 17 and 18) with a typical diameter of about 2–3 nm were used in this study. In principle, many FETs can be fabricated using a single SWCNT affording uniform performance.[12] SWCNTs were grown on degenerately *n*-doped Si wafer by chemical vapor deposition (CVD) and the wafer was covered with a layer of 100 nm thermal SiO_2. After CNT growth, the position of the CNT was located and Al_2O_3 film was grown on top of the CNT channel as defined by electron beam lithography and lift-off. The source (*S*), drain (*D*), and gate (*G*) electrodes (Pd or Al) were then fabricated using the same technique, as shown schematically in Fig. 1.

In this work we choose Al_2O_3 as the top-gate oxide for its wide band gap and good thermodynamic stability on Si. The performance of Al_2O_3 as gate oxide was explored earlier by IBM group.[12] Complementary inverters with gain of about 1 were fabricated and five of them were integrated into a ring oscillator. In this work Al_2O_3 thin film was first grown by electron beam deposition of Al_2O_3 source material di-

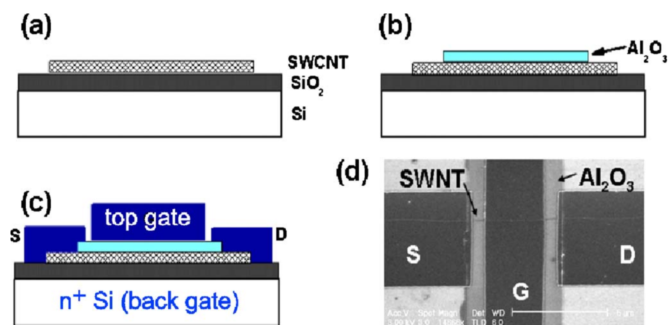

FIG. 1. (Color online) Fabrication process of top-gate CNTFETs. (a) SWCNT was first grown on SiO_2 substrate by CVD method, (b) an Al_2O_3 gate insulator layer was then grown on top of the SWCNT, (c) the source, drain, and gate electrodes were patterned by electron beam lithography and lift-off. (d) SEM image showing a typical so fabricated top-gate CNTFET.

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rectly. However, it was found that with this directly grown Al_2O_3 as the top-gate oxide, CNTFETs show hardly any field-effect for both the top-gate and back-gate voltage variations. The directly deposited Al_2O_3 film was found to be very rough, and corresponding gate leakage current was found to be not negligible unless the film thickness exceeds 100 nm. This is partly because during the electron beam deposition process, the temperature at the Al_2O_3 crucible is very high so that Al_2O_3 may have partially decomposed and the deposited film is therefore not stoichiometric Al_2O_3. The directly grown Al_2O_3 thin film may contain a large quantity of charge centers screening field modulation from both the top and back gates. In addition, the directly deposited Al_2O_3 film is not as compact as natural Al_2O_3 and contains many pin holes in the film leading to large gate leakage. In principle, this problem can be solved by post-high-temperature annealing (around 900 °C). However, we found that such a high temperature annealing will damage CNTs leading to device failure.

It is well known that there exists a layer of natural Al_2O_3 on metal Al surface, and this oxide layer is very thin but very compact and being able to prevent the metal Al from further oxidation. This thin Al_2O_3 layer has been proven to be good gate oxide for CNTFETs in bottom-gate configuration.[2,19] Noting that the natural Al_2O_3 film is usually about 3–4 nm thick, we therefore choose to first deposit Al film on top of the CNT with a nominal thickness of 2 nm and then oxidate it in water rich oxygen for 1 h at 130 °C. Usually, an Al film of 1–2 nm is not continuous even after oxidation. We therefore repeat such a deposition and oxidation processes several times to obtain a thicker and more uniform Al_2O_3 film. Quantitative atomic force microscopy examinations of the film revealed that the so grown film has a surface roughness of less than 1 nm. Electrical measurements show that the gate leakage current may be reduced below 1 pA for a 15 nm thick Al_2O_3 film.

When choosing Pd as the material for electrodes, the electrode forms an Ohmic contact or a low barrier Schottky contact with the valence band of the CNT leading to *p*-type CNTFETs.[4] On the other hand, using Al as the doping source may result in *n*-type CNTFETs, although it was found that this technique works only when the electrode was fabricated in high vacuum (10^{-8} torr) using sputtering technique and all measurements were carried out in vacuum.[8] In our experiments we found that after the growth of the top Al_2O_3 gate oxide all CNTFETs (either contacted using Pd or Al electrodes) shown *n*-type characteristics, and the I_{on}/I_{off} ratio for the top-gate geometry is much lower than that for the back-gate geometry. Since the Al_2O_3 film growth began with the deposition of Al on top of the CNT, the deposited Al atoms may first dope the CNT with electrons before being oxidized, and this may explain the *n*-type characteristics of the as fabricated CNTFETs.[8] It should be noted that the Al_2O_3 film was grown layer by layer and there must exist some interface states or charges in the film or at the interface leading to the reduction of the field effect of the as fabricated CNTFETs. It was found that the performance of the devices may be significantly improved by subsequent annealing of the grown Al_2O_3 film in Ar at 400 °C for about half an hour, while without damaging the CNT beneath the Al_2O_3 film. After annealing high performance *p*-type CNTFETs were obtained for Pd contacted CNTs, as shown in Fig. 2(a) and stable *n*-type CNTFETs were obtained for Al contacted CNTs, as shown in Fig. 2(b). Typically, the performance of the *n*-type CNTFETs is not as good as that of the *p*-type CNTFETs, e.g., the I_{on}/I_{off} ratio for *n*-type CNTFET is typically 10^2, while for *p*-type CNTFETs this ratio is more than 10^4. The higher performance of *p*-type CNTFETs results largely from the fact that excellent Ohmic contact forms between Pd and the valence band of CNT. Because the surface state pinning of the Fermi level at the metal/CNT interface is not firm, in principle, a suitable low work function metal may be used to form an Ohmic contact with the conduction band of the CNT, leading to near ballistic *n*-type CNTFETs. But up to now such an ideal *n*-type CNTFET has not been realized. The Al electrode forms a low barrier contact with the conduction band of the CNT, but not an ideal Ohmic contact.

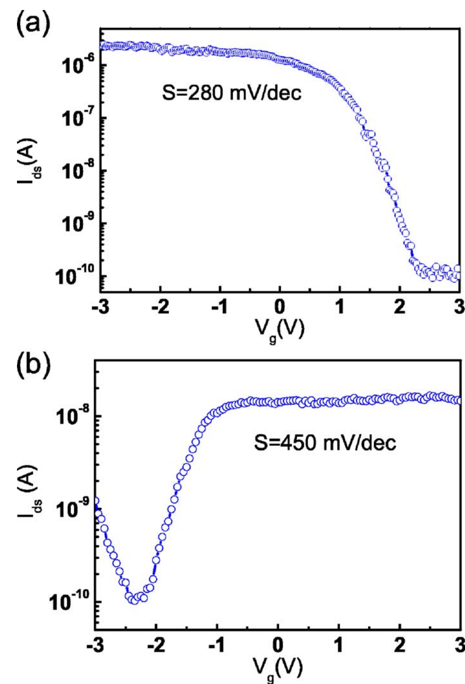

FIG. 2. (Color online) Transfer characteristics for (a) a *p*-type and (b) a *n*-type top-gate CNTFETs with 15 nm thick Al_2O_3 dielectric after annealing at 400 °C for half an hour.

Figure 3 compares the gate transfer characteristics of a typical *p*-type CNTFET for the top- and back-gate geometries. This figure shows clearly that the top-gate efficiency is significantly improved compared to that for the back gate. While the subthreshold swing S for the back gate is about 1.5 V/decade, it is only 750 mV/decade for the top-gate ge-

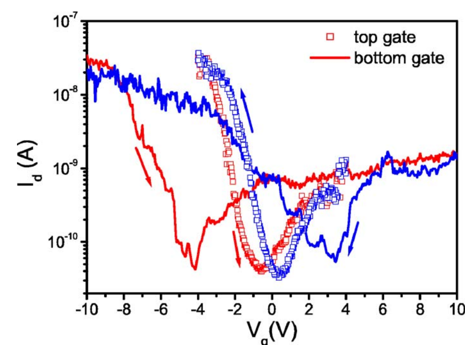

FIG. 3. (Color online) Gate voltage characteristics for both the Si back-gate (□) and top-gate geometries (–). The red curves were obtained by varying V_G from negative to positive and the blue curves from positive to negative.

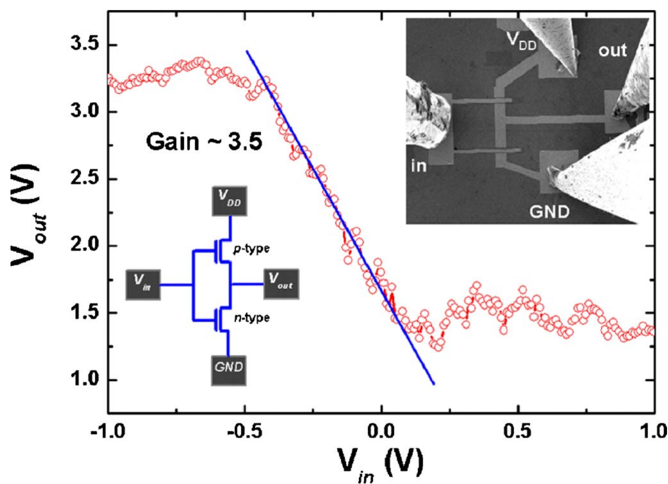

FIG. 4. (Color online) Transfer characteristics of a complementary voltage inverter fabricated using a single CNT, showing a gain of ~3.5. The upper right inset is a SEM image of the inverter.

ometry. The threshold voltage hysteresis in the gate transfer characteristics is also reduced significantly from about 8 V for the back-gate geometry to less than 1 V for the top-gate geometry, and this improvement is crucial for integrating separate devices into circuits. One such an example is the complementary inverter as shown in the insert of Fig. 4.

A particular useful device for digital applications is a combination of n- and p-channel metal-oxide semiconductor (MOS) transistors on adjacent regions, and this complementary MOS (commonly called CMOS) combination is realized when a p-type and n-type CNTFETs were fabricated side by side using the same CNT and controlled by a common gate voltage. An important feature resulting from the CNT band structure is that there is only one effective mass of carrier in CNT which is the same for both holes and electrons leading to near symmetric hole and electron transport, while the effective electron mobility in Si is roughly twice that of the hole mobility, making the design and fabrication of CMOS circuits more complicated. Shown in Fig. 4 is the transfer characteristics of the inverter, and a scanning electron microscopy (SEM) image of this inverter being tested using four probes is shown in the upper right inset of Fig. 4. These voltage characteristics show clearly a linear region between $V_g=-0.5$ and 0 V, yielding a gain of about 3.5 for this complementary inverter.

In conclusion, we demonstrated a simple process for fabricating stable p-type and n-type top-gate CNTFETs with Al_2O_3 being the gate oxide. The performance of the top-gate CNTFETs is shown to be much better than that of corresponding back-gate CNTFETs, and high performance complementary inverters with gain of about 3.5 are obtained by integrating the p- and n-type CNTFETs fabricated on the same SWCNT.

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