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Fabrication of silicon-based multilevel nanostructures via scanning probe oxidation and anisotropic wet etching

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Abstract
A rational approach is described for fabricating multilevel silicon-based nanostructures via scanning probe oxidation (SPO) and anisotropic wet etching. Using silicon oxide nanopatterns on Si(100) and Si(110) surfaces created by SPO as masks, two-dimensional (2D) nanostructures with high aspect ratio and a variety of patterns can be formed by anisotropic wet etching with KOH. By employing a mixture of KOH solutions and isopropyl alcohol (IPA) as an alternative to KOH alone, control of the morphology of the etched silicon surfaces, crucial for further fabrication, was greatly improved. The SPO and etching processes can be continually repeated on the 2D nanostructures, permitting the formation of various multilevel silicon-based nanostructures, including a T-gate structure useful for electronic circuitry. In addition, these multilevel silicon structures can be used as nanoimprint moulds for their rapid replication.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The present work demonstrates a technique for the fabrication of multilevel silicon-based nanostructures which involves the production of nanoimprint moulds for their rapid replication. Fabrication of multilevel nanostructures, especially those that are silicon-based, has attracted considerable attention owing to their great potential application in many fields, for example, in micro/nano-electromechanical systems (MEMS, NEMS), micro/nano-fluidic devices and micro/nano-optics [1–3]. In the search for methods for multilevel structuring at the sub-micron scale, several lithographic techniques, including electron beam lithography (EBL) [4–6], x-ray lithography (XRL) [7, 8] and focused ion beam (FIB) lithography [9] have been explored. However, the application of such methods is restricted because of their inherent limitations, which include complex systems and processing as well as their high cost. Recently, nanoimprint lithography (NIL) [10, 11] has emerged as a promising solution to this problem, with the advantages of high resolution, mass production and low cost. While offering great potential, the fabrication of multilevel nanostructures by NIL based on a multilayer resist system [12, 13] is still in its infancy because of the limitations in alignment technology and spatial resolution [14].

In recent years, many reports have focused on structural fabrication based on scanning probe lithography (SPL) [15–17]. Since the pioneering work [18] of the tip-induced local oxidation of an H-passivated Si surface using a scanning tunnelling microscope (STM) in ambient air, it has been demonstrated as a promising method to perform nanometre-scale lithography and widely applied to pattern semiconductors [19], metals [20], and organic thin films [21]. Based on SPL on an H-passivated silicon surface by an STM, Sakurai *et al* [22] reported Ag adsorption at the atomic

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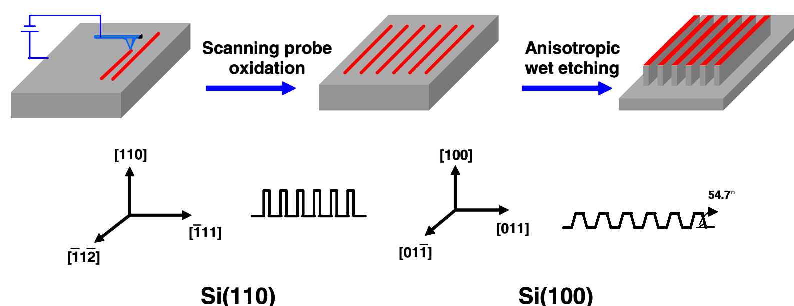


Scheme 1. Schematic illustration for the process and the orientation selection of ridge fabrication on Si(110) and Si(100) surfaces.

scale, and O'Brien *et al* [23] demonstrated the possibility of fabricating an atomically precise linear array of single phosphorus bearing molecules on a silicon surface.

Among various SPL techniques, scanning probe oxidation (SPO) [24] is the most promising, with the advantages that there is no need for a resist layer, and the method gives direct-writing, and high resolution (<50 nm). The process of local oxidation is similar to conventional electrochemical anodization where the STM/AFM tip is used as the cathode and water from ambient humidity is used as the electrolyte. The oxidation mechanism, especially when silicon is used as the sample, has been extensively studied [25–27]. When a positive bias voltage is applied to the silicon surface with respect to the conductive probe, high-resolution silicon oxide nanopatterns can be obtained, whose line-width and height can be easily controlled by changing the experimental conditions such as scan speed, tip bias, ambient humidity, tip type and tip diameter.

KOH-based silicon anisotropic wet chemical etching has also been known for a long time. This exploits the fact that the etching of {111} silicon crystal planes in KOH solution is very slow compared with {110} and {100} planes [28, 29]. Using scanning probe oxidation to produce a mask composed of nano-oxides, novel shaped patterns with high aspect ratio may be formed by subsequent anisotropic wet etching. Because of its inherent simplicity, generality and low cost, this method is widely used in 2D nanostructure fabrication and is regarded as an important technique for the simple preparation of nanometre scale devices [28, 30]. The high resolution and precise positioning ability of scanning probe microscopy (SPM) also raised the possibility of performing further fabrication on already patterned silicon wafers to generate pre-designed multilevel nanostructures. Chien *et al* [30] have succeeded in demonstrating multilevel structure fabrication by a combination of optical lithography and SPL. For most applications on future devices, it is highly desirable to fabricate the nanostructures with a more controllable and accurate method.

The approach described here for fabricating silicon-based multilevel nanostructures comprises three principal steps: (1) fabrication of 2D nanostructures on a silicon surface; (2) decreasing the surface roughness; and (3) fabrication of multilevel nanostructures on patterned 2D silicon surfaces. These multilevel silicon structures can also be used as NIL moulds for their rapid replication.

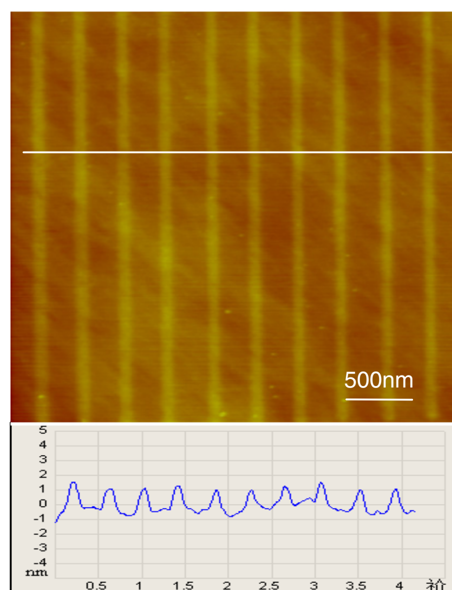


Figure 1. AFM image and section profile of an oxide pattern obtained by SPO on an Si(110) surface; the tip bias is −10 V and the scanning rate is 1 μm s^{-1}. The line width is about 100 nm and the period is 400 nm. The height data scale of the AFM image is 20 nm.

2. Fabrication of 2D silicon-based nanostructures on silicon substrates

Scheme 1 shows a schematic illustration for fabricating parallel ridges on silicon wafers by scanning probe lithography and anisotropic wet chemical etching. The silicon wafers used in this work were p-type Si(110) or Si(100) wafers with a resistivitly of 10–20 Ω cm. Before oxidation, the wafers were cleaned by Piranha solution (H_2SO_4/H_2O_2 = 7:3 (volume), at 90 °C) and then dipped in 1% HF (aq) to obtain a clean H-passivated silicon surface. A bias voltage was then applied to the SPM tip and the tip was scanned in trajectories parallel to one of the wafer ridges. Thus pre-designed linear oxide nanopatterns were formed on the Si surface. The SPO process was performed under ambient conditions (relative humidity ∼60%) with a commercial SPM (Dimension 3100, Digital Instrument Corporation). A typical oxide nanopattern fabricated by SPO is shown in figure 1.

Using the oxide nanopatterns as etching masks, wet KOH etching (20 wt% KOH) was used to generate ridges with vertical sidewalls on Si(110) and ridges with inclined sidewalls on Si(100).

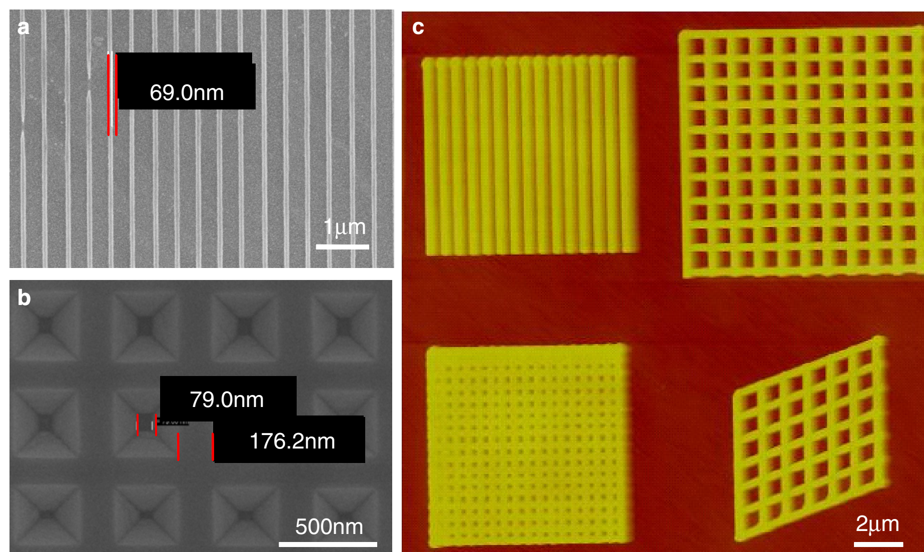


Figure 2. (a) SEM image of 70 nm width/400 nm pitch ridges on an Si(110) wafer; (b) SEM image of 500 nm pitch inverted pyramid pits on an Si(100) wafer; (c) AFM image of the nanostructure containing four difference type patterns; the height data scale is 200 nm.

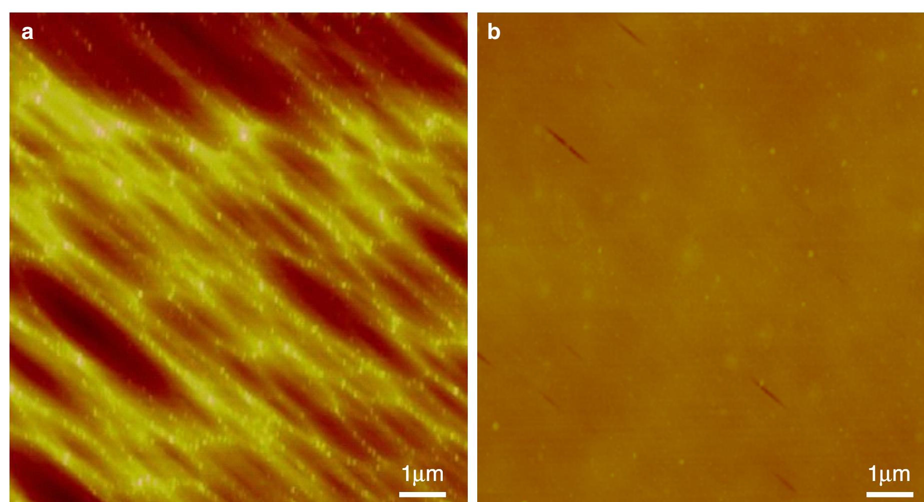


Figure 3. AFM images of the etched silicon surface. The height data scale is 100 nm. (a) Etched in 20 wt% KOH solution at 50 °C for 80 s, $R_q = 12$ nm; (b) etched in 20 wt% KOH + IPA solution at 50 °C for 80 s, $R_q = 1$ nm.

Figure 2(a) shows a scanning electron micrograph (SEM) image of the ridges on an Si(110) surface fabricated by SPO (tip bias $= -6$ V, scan speed $= 40$ μm s^{-1}) and following wet etching (in 20 wt% KOH for 20 s at 50 °C), which have a period of 400 nm. As denoted in scheme 1, in the case of Si(110), the oxide line is intentionally oriented along the $\langle 112 \rangle$ direction, which is parallel with one of the $\{111\}$ crystal planes normal to the (110) silicon surface. According to the etching selectivity between different crystal planes of silicon, lines in this direction gave ridges with vertical sidewalls. The ridges have a 70 nm line width and a height of about 100 nm.

The oxide mask patterns are not limited to lines; grids of various patterns can also be written on to the silicon surface, which may in turn be developed into novel structures by wet chemical etching. The crystal orientation in the case of Si(100) and the resulting pattern section are also shown in scheme 1. Because $\{111\}$ planes are not vertical to the (100) surface, inclined sidewalls will be formed. Therefore, based on the orientation of the Si(100) planes, V-shape grooves, inverted trapezium-shaped grooves and pyramidal pits can be routinely fabricated by a combination of SPO and anisotropic wet etching. Figure 2(b) shows a scanning electron micrograph (SEM) image of pyramidal pits fabricated on Si(100) wafers. The line width is about 175 nm and their period is 500 nm. Figure 2(c) shows an AFM image of the structure on an Si(110) wafer which is composed of four different patterns with a central distance of 10 μm. It proves the flexibility of this method, which is offered by the characteristics of atomic force microscopy.

Aimed at the ability to obtain different structures with specific features, we studied the oxide line width dependence on oxidizing conditions such as AFM probe type, bias voltage, tip–sample distance and duration of oxidation. The most important of these are the properties of the probe. The line width and their uniformity greatly depend on aspects of the probe, such as probe material, geometry, coating layer,

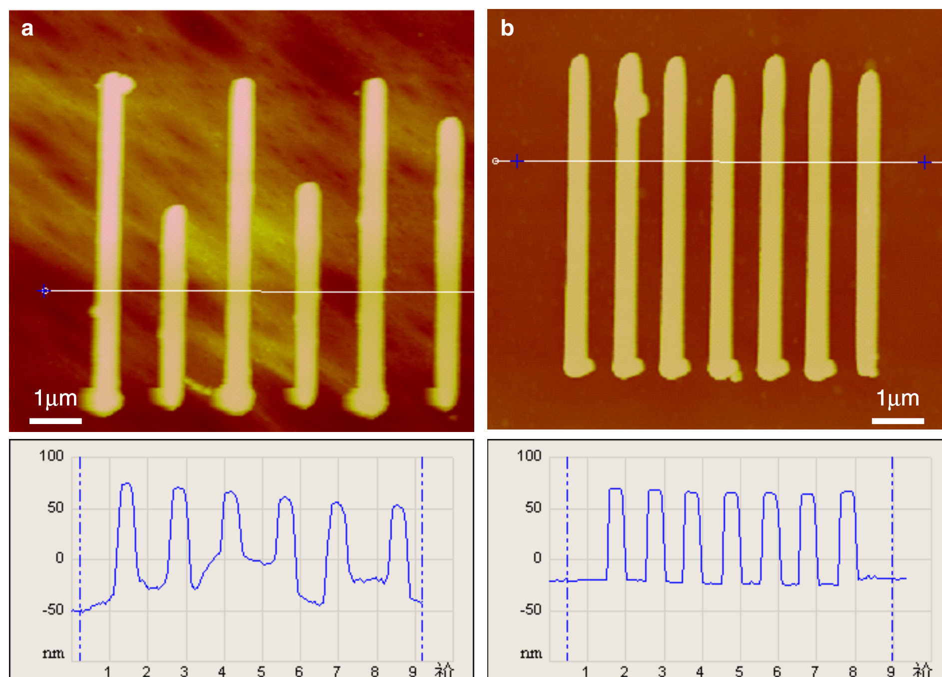


Figure 4. AFM images and section profile images of the ridges. The height data scale is 200 nm. (a) The etchant is KOH solution; (b) the etchant is KOH + IPA solution.

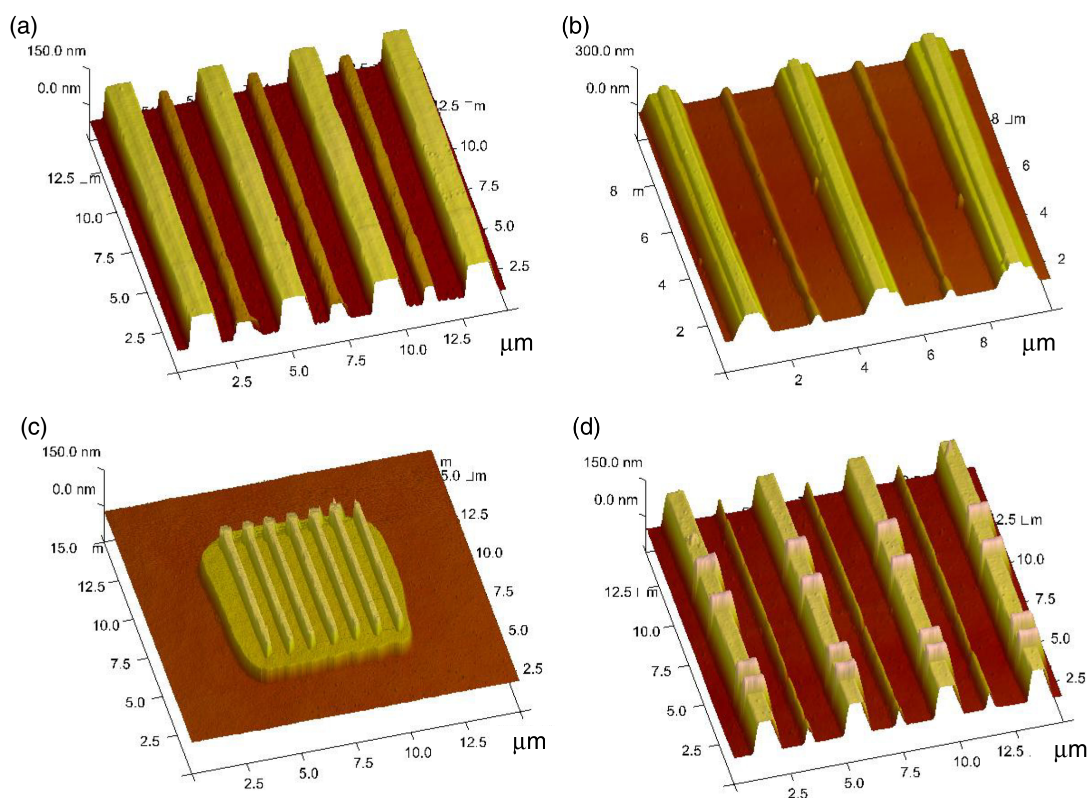


Figure 5. AFM images of several kinds of multilevel silicon structures.

and their thickness. This is consistent with the proposed oxidation mechanism where the local electric field between the sample and the tip plays a crucial role, since the tip shape and its conductivity determine the electrical field distribution. Also, the lifetime of these conductive probes is quite different due to their distinct materials or coating layer. The probes investigated in this study included highly doped silicon probes (NSC11/50, Ultra-Sharp Corporation, Russia), TiN coated silicon probes, Co/Cr coated silicon probes (MESP21282, Digital Instrument Corporation), and Pt–Ir coated silicon

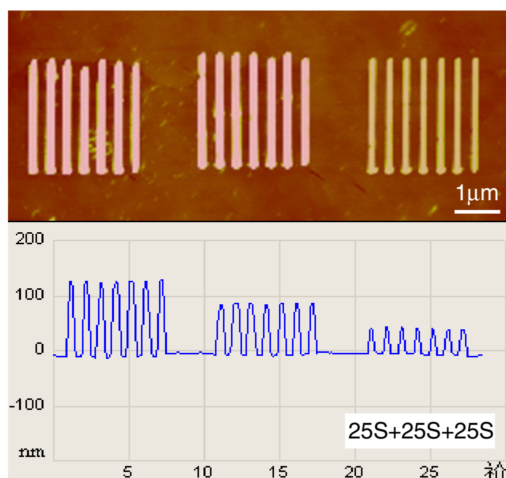


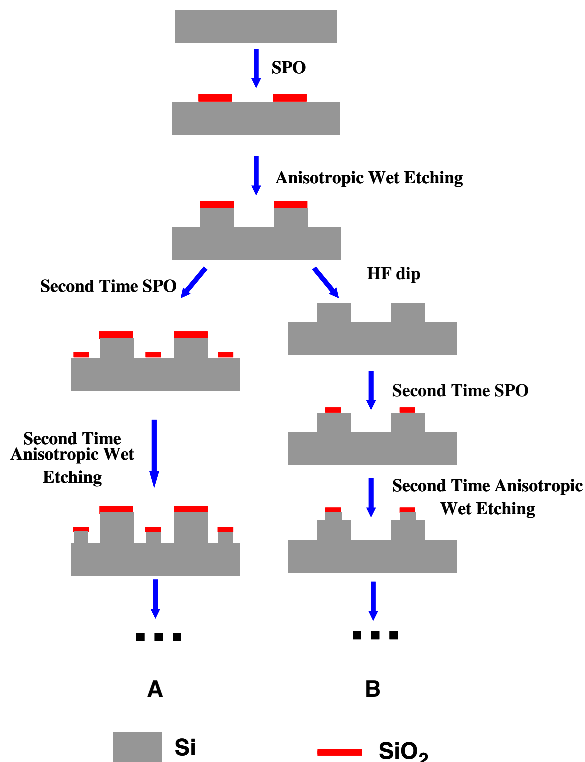
Figure 6. AFM image and the section profile of a silicon structure which was formed by a three times oxidation and etching process; the height of the ridges from left to right is 135, 90, 45 nm, respectively.

probes (Digital Instrument Corporation). The best results were obtained when using Co/Cr coated silicon probes in tapping mode, which provided highly consistent repeatable oxidation patterns at high resolution. With regard to repeatability, it is important to note that, after several hundred oxidation cycles, probes will become blunt and can produce oxide lines with widths even greater than 1 μm. The line width is also sensitive to tip bias and tip–sample distance. Increasing the tip bias or shortening the distance always produced increased line width.

3. Decreasing the surface roughness

At first, we attempted to fabricate multilevel nanostructures on the 2D structures created by SPO and KOH-based silicon anisotropic wet chemical etching. However, the second nanofabrication step on the KOH etched silicon was extremely difficult due to considerable surface irregularity. Figure 3(a) shows an AFM image of the silicon surface which was etched at 50 °C using 20 wt% KOH solution for 80 s. The mean square roughness (R_q) of this surface was about 12 nm. This was far larger than the height of the scanning probe oxidation induced nanopatterns themselves (typically 2–3 nm). To improve the surface morphology, it was necessary to develop a better etching system. It has been mentioned by Chien *et al* [30] that a mixture of tetramethyl ammonium hydroxide (TMAH) and isopropyl alcohol (IPA) solutions will improve the smoothness of the etched surface. This etchant has been used in our study and resulted in a surface R_q of about 3 nm, which is still not ideal. In our experiment, a mixture of 20 wt% KOH and IPA (volume ratio = 5:1) was used as etchant instead of 20 wt% KOH. It was suggested that the IPA might compete with KOH for binding sites at the solid–liquid interface and result in the reduction of etching rate [31]. At the same time, the IPA will act as a surfactant and reduce the adherence of bubbles and the precipitation of SiO_2 to the silicon surface [32]. Figure 3(b) shows an AFM image of the silicon surface, which has a surface R_q of only about 1 nm, after etching in KOH/IPA at 50 °C for 80 s.

We also compared the section profiles of patterns produced by these two different etchants; see in figure 4. The heights of these two patterns are both around 100 nm, but as can be seen from these pictures, there are considerable differences between their surface morphologies. Using KOH alone (figure 4(a)) produced an uneven undercutting and a variable height with the maximum vertical distance between the grooves of about 40 nm. In contrast, when KOH/IPA was used, a very good reproducible pattern was obtained with a maximum vertical distance between grooves of less than 2 nm. From these comparisons, it is clear that the KOH/IPA mixed etching system produces excellent results, with low surface irregularity and uniform surface features. Using this alternative etching system, further fabrication on the already etched structures was successfully carried out and produced multilevel nanostructures on both Si(110) and Si(100).



Scheme 2. Schematic flowchart of the fabrication of multilevel silicon nanostructures.

4. Fabrication of multilevel nanostructures on silicon surfaces

Scheme 2 illustrates the multilevel structure fabrication process. First, a 2D silicon nanostructure is fabricated using SPO oxidation and wet etching, leaving a SiO_2 pattern in place on the silicon surface. This 2D template can be used in one of two ways. First, using further scanning probe oxidation and wet etching directly on this 2D structure, new oxide patterns beside previous produced ones can be generated by second time SPO and used as an etching mask. So patterns with different heights can be formed. We designated these structures type A. Second, we can carry out an HF dipping process to remove the oxide layers produced in the first SPO, and then carry out a second SPO/etching process. This was designated type B. Further multilevel structures can be obtained by repeating the

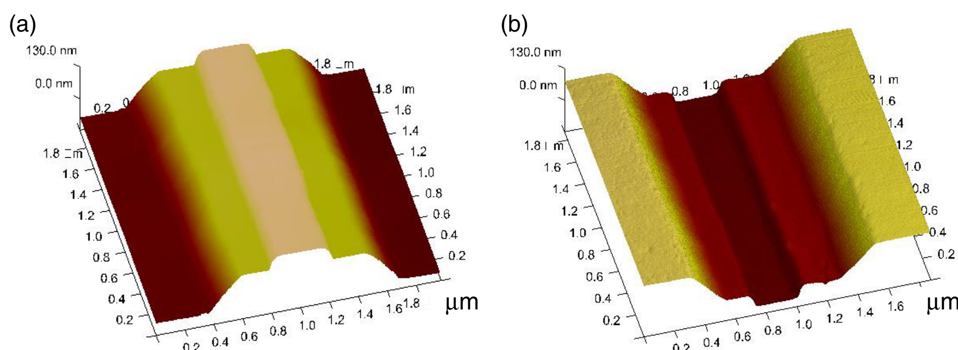


Figure 7. (a) 3D AFM image of a nanostructure fabricated by scanning probe oxidation and anisotropic wet etching; (b) 3D AFM image of the nanostructure obtained by nanoimprint lithography using (a) as the mould.

process. By choosing different fabrication routes, multilevel patterns with different heights on one plane and stacked structures or assembled structures can be produced.

Figure 5 shows four examples of multilevel silicon nanostructures fabricated by this method. The anisotropic etching processes were all performed in the KOH/IPA system. The structure shown in figure 5(a) was fabricated on an Si(100) wafer, which underwent the process illustrated in scheme 2. Its first and second oxidation procedures were performed using the same tip with a different tip bias, −10 and −8 V respectively, and a wet etching duration of 25 s. Two ridge types can be seen; the wider one has a width of about 900 nm and a height of 130 nm. The corresponding values of the thinner ridge are 250 nm and 66 nm respectively. Repeating scheme 2 on the structure shown in figure 5(a), we obtained the structure shown in figure 5(b). A thinner ridge with 250 nm width and 52 nm height was fabricated on the 900 nm wide ridges. A magnified image of this stacked structure is shown in figure 7(a). It is a T-shaped gate structure, which been widely used in the electronics industry. Figures 5(c) and (d) were two other stacked structures. From these examples it can be deduced that a very wide range of multilevel structures can be fabricated. To examine the controllability and the repeatability of this fabrication method, we repeated an identical oxidation and wet etching process three times on the same silicon wafer and obtained the result shown in figure 6. From this we can see that the relative location and height of the patterns formed in different fabrication cycles can be precisely controlled. All the characteristics of this fabrication method mentioned above ensure its great potential of application both in research and in industry.

5. Replication of multilevel nanostructures by NIL

Despite all the advantages of this method, it does not have mass-production potential, due to the inherent relatively low speed of AFM. And additionally, the multilevel structure material was restricted to a specific silicon wafer. To overcome these shortcomings, we looked at the possibility of replicating these structures by imprint transfer. Nano-imprint lithography (NIL) is a mass-production, low-cost structuring technology that was proposed by Chou in 1995 [11]. Its basic mechanism is using a rigid mould to imprint on a polymer layer pre-coated on the choice substrate. The patterns on the mould are thus transferred to the polymer layer and can be further transferred to the substrate by reactive ion etching (RIE) and lift-off. Therefore, using the multilevel silicon structures fabricated by this approach as NIL moulds, we may get multilevel structures by single-step NIL. Figure 7 shows our preliminary NIL results. The imprinting was performed on a PMMA ($T_g = 122\,^{\circ}$C) polymer layer pre-coated on a silicon substrate at a temperature of 190 °C and a pressure of 40 bar for 2 min. Figures 7(a) and (b) are the AFM images of the structures on the mould and polymer respectively. As can be seen from them, the T-shaped gate structure has been faithfully replicated. These structures can also be transferred to other materials by RIE and lift-off. As is widely appreciated, one of the great challenges existing in NIL technology is the problem of alignment between different layers, which renders it inconvenient to fabricate multilevel nanostructures by NIL. However, by using a multilevel structure as a mould, we can get complicated nanostructures whose dimensions and geometry can be precisely controlled. This single-step NIL eliminates the alignment issue and provides a rapid and faithful multilevel structure replication approach.

6. Summary

In summary, we have presented a rapid, flexible and reproducible means for multilevel structure construction. By employing scanning probe oxidation and silicon-based anisotropic wet chemical etching, we are able to produce nanometre structures with controllable dimensions and geometry. By adding IPA to the KOH wet etching solution, we obtained decreased surface root mean roughness and very good structure uniformity. Based on this optimized etchant, we succeeded in performing repeated oxidation and etching processes on one wafer and obtained multilevel silicon nanostructures including T-shaped gate structure. Due to the high resolution and precise positioning of AFM, a whole range of structures may be designed and fabricated easily by this means. This provides a versatile method for fabricating multilevel structures, which will be greatly beneficial to both scientific research and electronic industrial development. Additionally, these multilevel structures were succeeded replicated by single-step NIL, which eliminates the alignment issue exiting in current multilevel fabrication technique and sheds light on rapid fabrication of multilevel nanostructures.

Acknowledgments

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