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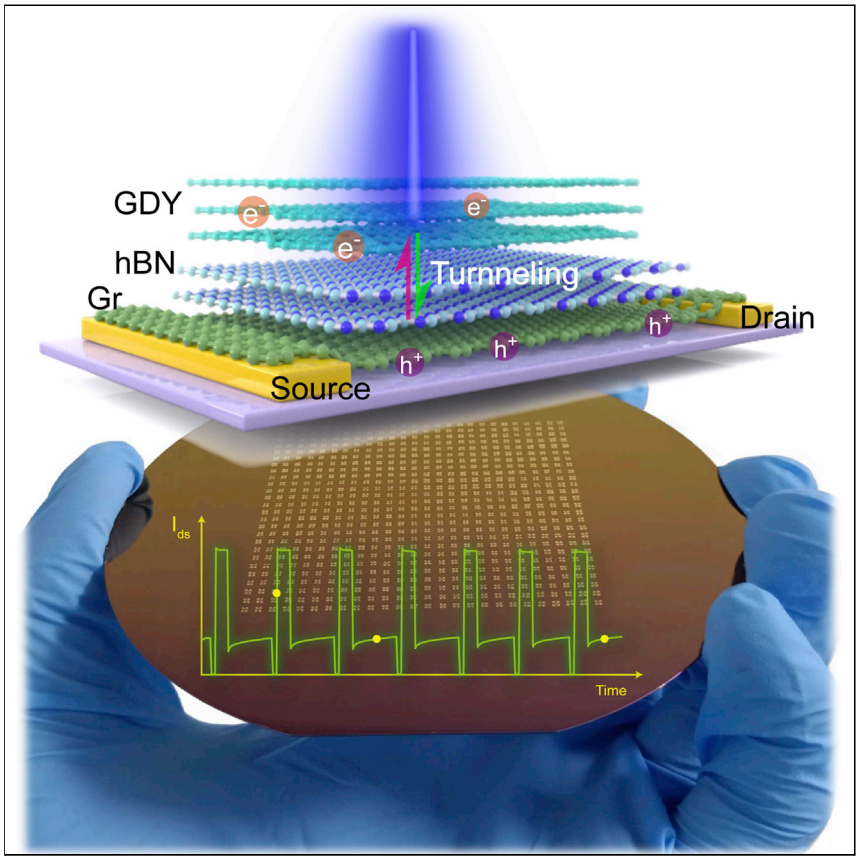

A wafer-scale graphdiyne (GDY) film with 1 nm thickness, high crystalline, and uniformity is synthesized via an electric double-layer-confined strategy. Then, a two-terminal top-floating-gated optoelectronic memory is fabricated using GDY as a photoresponsive top-floating gate. Benefiting from the excellent charge storage capability and high photoresponse of GDY, the memory presents multibit storage capability with over 256 distinct storage levels and flexibility with over 1,000 bending circles.

Jiaqiang Li, Zhicheng Zhang, Ya Kong, ..., Xudong Chen, Tongbu Lu, Jin Zhang

chenxd@email.tjut.edu.cn (X.C.)
jinzhang@pku.edu.cn (J.Z.)

HIGHLIGHTS

A wafer-scale graphdiyne film with high quality is synthesized

An optoelectronic flash memory is fabricated using graphdiyne as a top-floating gate

The graphdiyne-based memory presents flexibility and multibit storage capability

Li et al., Chem 7, 1–13
May 13, 2021
https://doi.org/10.1016/j.chempr.2021.01.021

Please cite this article in press as: Li et al., Synthesis of wafer-scale ultrathin graphdiyne for flexible optoelectronic memory with over 256 storage levels, Chem (2021), https://doi.org/10.1016/j.chempr.2021.01.021

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Synthesis of wafer-scale ultrathin graphdiyne for flexible optoelectronic memory with over 256 storage levels

Jiaqiang Li,[1,3] Zhicheng Zhang,[2] Ya Kong,[1] Binwei Yao,[2] Chen Yin,[1,4] Lianming Tong,[1] Xudong Chen,[2,*] Tongbu Lu,[2] and Jin Zhang[1,5,*]

SUMMARY

Two-dimensional (2D) graphdiyne (GDY) is a promising floating-gate material for flexible optoelectronic flash memory owing to its fascinating electrical and optical properties. However, research in GDY-based flash memory is still in its infancy owing to the huge challenge in the synthesis of large-area and ultrathin GDY films with high quality and uniformity. Here, an electric double-layer-confined strategy is proposed to synthesize a wafer-scale GDY film with thickness of 1 nm. Then, a two-terminal top-floating-gated optoelectronic memory with multibit storage capability is investigated using GDY as a photoresponsive top-floating gate. Benefiting from the excellent charge storage capability and high photoresponse of GDY, this device exhibits over 256 distinct storage levels (8 bits) with signal-to-noise ratios larger than 100. Moreover, the fully 2D material and two-terminal architecture endows the device with robust bending stability for over 1,000 bending circles, paving the way to develop wearable electronics.

INTRODUCTION

It was predicted that more than 44 × 10^{12} GB data would be generated in 2020,[1] which requires a huge memory to store these ever-growing data. As the most mature nonvolatile memory for low-cost massive data storage, conventional silicon-based flash memory has encountered its bottleneck with the continuous scaling down of the device size, especially the dramatical degradation of the gate-coupling ratio (GCR) and strong cell-to-cell interference (CTCI) for floating gate (heavily doped polysilicon).[2,3] In recent years, flash memories with innovative device architectures and novel materials have been intensively investigated to improve the figures of merit, in which two-dimensional (2D) materials exhibit unique advantages owing to their extraordinary properties.[4–6] As a newly emerging carbon allotrope, graphdiyne (GDY) exhibits fascinating electrical and optical properties.[7–10] Especially, the high density of states (DOSs), large work function (WF), and low dimensionality[11,12] make GDY a promising floating-gate material for flash memory, since GDY can store more charge and suppress the GCR degradation and CTCI in comparison with conventional floating-gate materials. Moreover, the natural band gaps and strong optical absorption enable GDY to be applied as a photoresponsive floating gate in optoelectronic memory, and the π-conjugated 2D planar network structure and strong mechanical strength endow GDY with greater flexibility than conventional 2D materials such as MoS_2,[13–16] facilitating the development of flexible flash memory to be integrated in wearable systems.

The bigger picture

Recently, 2D-material-based flash memories with innovative device architectures and novel materials have been intensively investigated to break through the bottleneck of conventional silicon-based flash memory. As a new carbon allotrope, graphdiyne (GDY) exhibits fascinating electrical and optical properties, making GDY a promising floating-gate material for flash memory. However, great challenge in the synthesis of large-area and ultrathin GDY films with high quality hindered the development of GDY-based memory. Here, a novel strategy is proposed to synthesize a wafer-scale GDY film with thickness of 1 nm, and an optoelectronic memory with multibit storage capability is investigated using GDY as a photoresponsive top-floating gate. The device exhibits over 256 distinct storage levels with high signal-to-noise ratios. Moreover, the fully 2D-material and two-terminal architecture endows the device with robust bending stability, paving the way to develop wearable electronics.

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For practical applications of GDY in devices, it is essential to synthesize ultrathin film with large area and high quality in a simple and reliable way. In the past decade, tremendous efforts have been devoted to improve the scale and quality of the prepared GDY film since GDY was first prepared by Li et al. in 2010.[17–22] For example, space-confined strategies assisted by interfaces were proposed to synthesize GDY thin film,[18,19,22] and van der Waals epitaxial strategies were developed to synthesize few-layered crystalline GDY on graphene (Gr).[20,21] However, the GDY films synthesized by these methods cannot simultaneously possess the characteristics of large area, ultrathin, and high crystallinity; either they have the characteristics of large area but exhibit very large thickness, or they are ultrathin but have small domain size, or it is difficult to exfoliate them from template, which inevitably hinders their further application in devices.[19] Therefore, it is highly desirable to develop a reliable strategy that can synthesize large-area and high-quality GDY film with controllable thickness.

In this work, a novel electric double layer (EDL)-confined strategy was developed to synthesize few-layered GDY film with ABC stacking on Cu foil assisted by a DC electric field (EF). A wafer-scale GDY film with thickness of 1 nm was synthesized and paved the way to develop GDY-based flash memory. Here, a two-terminal multibit optoelectronic memory was constructed with a GDY/hexagonal boron nitride (hBN)/Gr heterostructure using GDY as a photoresponsive top-floating gate. Benefiting from the excellent charge storage capability of GDY, the device exhibits an unprecedented data storage capability with over 256 distinct storage levels (8 bits) with signal-to-noise ratios (SNRs) larger than 100 in the processes both of programming and erasing, far superior to the existing multibit memories.[23–27] Moreover, the fully 2D-material and two-terminal architecture endow the device with robust reliability and stability in bending test (over 1,000 bending cycles), providing a competitive solution for massive data storage in the future flexible and wearable electronics.

RESULTS AND DISCUSSION

Synthesis of wafer-scale GDY film via the EDL-confined strategy

The schematic illustration and experimental setup of the EDL-confined strategy are depicted in Figures 1A and S1, in which the copper foil and gold foil are connected to the cathode and anode of a DC EF, respectively. Dielectric acetone was used as electrolyte to avoid the oxidation/reduction reactions. Briefly, copper ions are released from the cathode (copper foil) to form catalytic complex in the presence of N,N,N′,N′-tetramethylethylenediamine (TMEDA),[28] and these catalytic copper ions are confined and uniformly distributed on the surface of cathode to form an EDL.[29,30] Consequently, the alkyne coupling only occurs in extremely thin EDL to form a few-layered GDY film with a large area. To demonstrate the mechanism of the EDL-confined strategy, a gold foil was used as a cathode, and catalytic copper ions were introduced manually (Figure S2). Driven by the external EF, copper ions moved to the cathode, and alkyne coupling reaction only occurred on the surface of cathode to form GDY film (Figures S2A–S2D), which was demonstrated by the scanning electron microscope (SEM) images and Raman spectra (Figures S2E–S2G).

For this EDL-confined strategy, EF plays a significant role in the formation of a layer-like GDY. As shown in Figure S3, a series of voltages (U) ranging from 1 to 4 V were used to synthesize the GDY film. The results show that the prepared GDY film was discrete for U = 1 V, whereas continuous films with high roughness were obtained for U = 3 and 4 V. The SEM images demonstrate that a GDY film with uniform and

[1]Center for Nanochemistry, Beijing Science and Engineering Center for Nanocarbons, Beijing National Laboratory for Molecular Sciences, College of Chemistry and Molecular Engineering, Peking University, Beijing 100871, P.R. China

[2]MOE International Joint Laboratory of Materials Microstructure, Institute for New Energy Materials and Low Carbon Technologies, School of Material Science and Engineering, Tianjin University of Technology, Tianjin 300384, P.R. China

[3]Advanced Membranes and Porous Materials Center, Physical Sciences and Engineering Division, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia

[4]Academy for Advanced Interdisciplinary Studies, Peking University, Beijing 100871, P.R. China

[5]Lead contact

*Correspondence: chenxd@email.tjut.edu.cn (X.C.), jinzhang@pku.edu.cn (J.Z.)

https://doi.org/10.1016/j.chempr.2021.01.021

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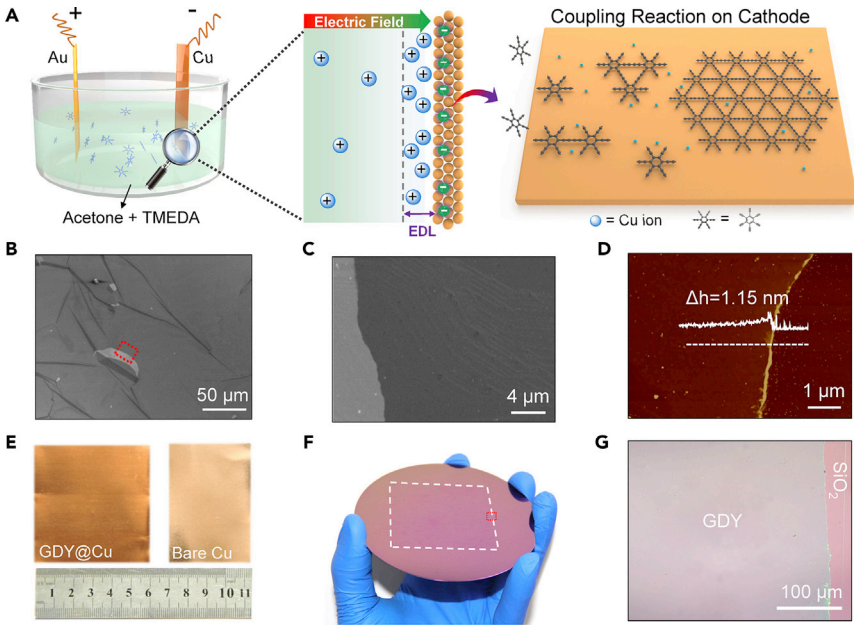

Figure 1. Schematic illustration of the experimental setup and characterization of GDY film

(A) Schematic illustration of the experimental setup and principle.

(B) SEM image of the few-layered GDY film on cathode (U = 2 V).

(C) Zoom in image of the selected area of (B).

(D) AFM image of few-layered GDY film.

(E) Photographs of cathode after reaction completed (GDY@Cu) and bare copper foil.

(F) Photograph and (G) OM image of the wafer-scale GDY film on SiO_2/Si wafer.

flat surface was synthesized with an optimum voltage of 2 V (Figures 1B and 1C). As a comparison, the morphology of the GDY film with $U = 0$ V presents a nanowall structure (Figure S4). Investigation of the copper concentrations in electrolyte under different voltage shows the copper concentration decreases along with increasing voltage (Figure S5), indicating that the copper ions absorbed on cathode increase along with the increasing voltage. The thickness of the prepared GDY film was investigated via atomic force microscope (AFM). Figure 1D indicates that a uniform GDY film with thickness of 1.15 nm was synthesized under an optimized hexaethynylbenzene (HEB) concentration (0.8 μg mL^{-1}), which can be regarded as a triple-layered GDY.[20] The statistical thickness data of the as-grown GDY film were extracted from 90 independent domains and exhibited a narrow distribution centered at 1.10 nm (Figure S6), which is close to that of a triple-layered GDY (1.05 nm, Figure S6 inset).[20] The thickness of the GDY film can be tuned (from 1.15 to 10.51 nm) by adjusting the concentration of HEB monomers (from 0.8 to 8 μg mL^{-1}, Figures S7A–S7C). In addition, discrete GDY fragments with average thickness of ~0.58 nm were obtained when HEB concentration decreased to 0.16 μg mL^{-1} (Figure S7D). This EDL-confined strategy provides a feasible route to prepare large-area GDY film with high uniformity. As shown in Figure 1E, a continuous and uniform GDY film was synthesized on a 6 × 6 cm copper foil. This GDY film was transferred onto a 4-inch SiO_2/Si wafer (Figure 1F), and the optical microscopy (OM) image reveals a clean and uniform surface (Figure 1G). This is the first strategy that can synthesize wafer-scale and high-crystallinity GDY films with thickness about 1 nm.

The quality and crystallinity of the prepared GDY film via the EDL-confined strategy were characterized. Figure 2A shows a typical Raman spectrum of GDY film grown on cathode with $U = 2$ V, in which distinct peaks at 1,376, 1,528, 1,583, and 2,174 cm^{-1}

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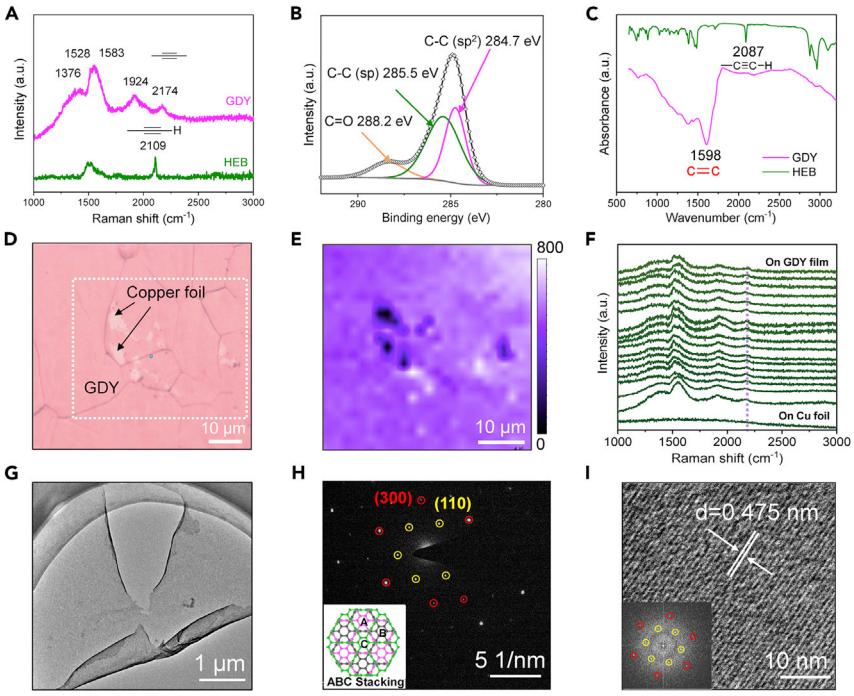

Figure 2. Structure characterization of GDY film

(A) Raman spectra of HEB and GDY on cathode when voltage is 2 V.

(B) XPS spectrum of GDY film: narrow scan for element C1s.

(C) FTIR spectra of GDY film and HEB.

(D) OM image of GDY film on copper foil.

(E) Integrated intensity Raman maps of C≡C triple bond (2,174 cm^{-1}) of GDY film over the area in (D), confirming the uniformity of the GDY film in macroscopic scales.

(F) Typical Raman spectra randomly collected across the corresponding sample in (D).

(G and H) (G) TEM image and (H) SAED pattern of few-layered GDY film. ABC stacked GDY model is shown in the inset.

(I) HRTEM image of few-layered GDY film. Corresponding FFT pattern of HRTEM image is shown in the inset.

are consistent with the typical bands of GDY.[10,20] The Raman shift of C≡C bond in GDY (2,174 cm^{-1}) presents a blueshift comparing with that in HEB (2,109 cm^{-1}) due to the formation of conjugated diyne linkages.[28] Comparison with Raman spectra of GDY films prepared at different DC voltages (0–4 V) implies that U = 2 V is an optimized voltage (Figure S8A). It is worth noting that the GDY film prepared at U = 2 V exhibits a minor C–Cu (II) complex intensity (1,924 cm^{-1}) compared with that synthesized at U = 0 V, (Figure S8B), indicating a higher degree of polymerization. X-ray photoelectron spectroscopy (XPS) measurements indicate that the GDY film is mainly composed of a carbon element (Figure S8C), and the C1s orbital at 285.0 eV can be deconvoluted into three sub-peaks at 284.7, 285.5, and 288.2 eV, which are assigned to the C=C, C≡C, and C=O bonds, respectively (Figure 2B). Energy-dispersive spectroscopy results indicate dominant carbon element is uniformly distributed over the whole film (Figure S9). Figure 2C shows the Fourier transform infrared (FTIR) spectrum of GDY, in which the band at 1,598 cm^{-1} can be attributed to the skeletal vibration of aromatic ring.[31] The disappearance of band at 2,087 cm^{-1} is ascribed to the typical stretching vibration of terminal alkyne, which demonstrates the formation of highly ordered diyne linkage with π conjugation.[32] The band gap of GDY film (0.90 eV) was obtained from the electron energy loss spectroscopy (EELS) spectrum in Figure S10A, which is very close to the predicated band gap (0.78 eV,

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Figure S10B). To demonstrate the uniformity of the prepared GDY film, Raman mapping was performed in the selected area of Figure 2D. Figures 2E and 2F show the Raman mapping image of C≡C bonds at 2,174 cm^{-1} and corresponding Raman spectra, indicating the high uniformity of GDY film.

The morphology of GDY is further confirmed by transmission electron microscope (TEM) (Figure 2G). Selected area electron diffraction (SAED) exhibits a typical hexagonal symmetric pattern (Figure 2H), demonstrating the high crystallinity of the GDY film. The innermost hexagonal spot series are indexed as a set of (110) diffractions derived from a hexagonal 2D lattice with a = b = 0.96 nm.[11,12] The SAED pattern is in good agreement with previous simulations, which revealed that the observed diffraction pattern matches exclusively that of ABC···-stacked GDY (Figure 2H inset) rather than AA···-stacked, AB···-stacked, or single-layered GDY.[18,20] Considering that the average thickness of GDY film is about 1.10 nm, a triple-layer GDY film with ABC-stacking structure can be concluded. As shown in Figure 2I, highly crystalline GDY domain with a lattice parameter of 0.475 nm was directly observed via high-resolution TEM (HRTEM), corresponding to the (110) plane of GDY.[20] The fast Fourier transformation (FFT) image of the HRTEM image also shows a typical hexagonal symmetric pattern (Figure 2I inset), which is in agreement with the SAED result.

Two-terminal nonvolatile optoelectronic memory

As mentioned above, GDY is a promising floating-gate material for flexible optoelectrical memory owing to its intrinsic properties, such as high DOS and WF, natural band gap, strong absorption, strong mechanical strength, and low dimensionality. Here, a two-terminal multibit optoelectronic memory with GDY/hBN/Gr heterostructure was constructed using GDY as a photoresponsive top-floating gate (Note S1). Compared with conventional flash memories with three-terminal architecture, two-terminal memory device without gate electrode will facilitate device miniaturization and therefore increase integration density.[33] Figure 3A illustrates the structure of the fabricated two-terminal optoelectronic memory, in which chemical vapor deposition (CVD)-grown monolayer graphene and hBN film (5 nm) act as the channel and tunneling barrier layer, respectively. As shown in Figure 3B, a 26 × 26 device array was fabricated on a 4-inch SiO_2/Si wafer using the prepared wafer-scale GDY film.

Figure 3C shows the dynamic behavior of the device in several switching cycles, including (1) programming, (2) on-current reading, (3) erasing, and (4) off-current reading processes. A negative $V_{ds\text{-}pro}$ pulse (–13 V, 10 s) was used to program the device from off state to on state, and in turn, the device will return to its initial state by applying a light pulse (450 nm, 30 mW cm^{-2}, 3 s). The mechanism of these four processes is illustrated in Figure 3D. A Vds-pro pulse of –13 V for 10 s is applied to program the device (Figure 3Di), which is much smaller than the programming voltage used in three-terminal memories.[23,24,27,34–36] Under this $V_{ds\text{-}pro}$ pulse bias, the Fermi level of graphene is elevated, and simultaneously, electrons from the drain would tunnel to GDY film through hBN barrier due to the large potential drop between drain and GDY.[6,33] These electrons are confined in GDY owing to the high WF of GDY and high hBN barrier. After programming, the V_{ds} is switched to 0.02 V for current reading ($V_{ds\text{-}read}$). At this stage, GDY film with trapped electrons can be regarded as a negatively charged top gate to graphene channel (Figure 3Dii), which will induce a significant increase of the drain current I_{ds} to 4 μA $μm^{-1}$. In the erasing process (Figure 3Diii), abundant electron-hole pairs are generated in GDY under illumination of a light pulse (450 nm, 30 mW cm^{-2}, 3 s) at V_{ds} = 0.02 V. Driven by the built-in EF between GDY and graphene, the photogenerated electrons tunnel

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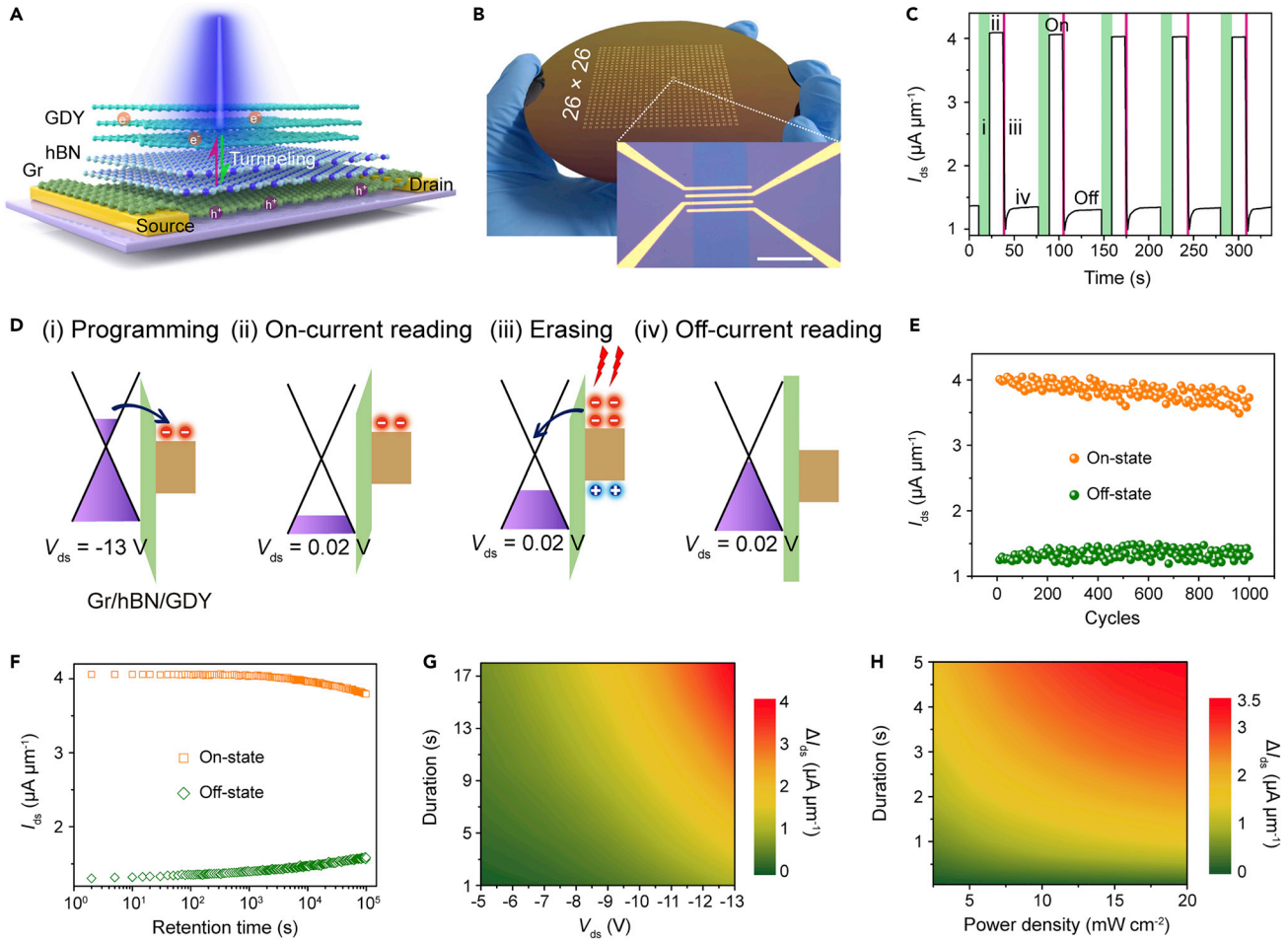

Figure 3. Two-terminal nonvolatile optoelectronic memory based on GDY/hBN/Gr heterostructure

(A) Schematic illustration of the two-terminal memory device.

(B) Photograph of a 26 × 26 device array on a 4-inch wafer. Each unit contains 3 independent devices. Inset is the OM image of the memory device with a channel length and width of 50 and 5 μm, respectively. Scale bar, 50 μm.

(C) Dynamic behavior of the memory in five P/E cycles with reading voltage of V_{ds} = 0.02 V. Programming process: a $V_{ds\text{-}pro}$ pulse of –13 V for 10 s (green region); erasing process: a 450-nm light pulse with intensity of 30 mW cm^{-2} at V_{ds} = 0.02 V for 3 s (pink region).

(D) Schematic illustration of the energy band diagram for (Di) electrical programming, (Dii) on-current reading, (Diii) optical erasing, and (Div) off-current reading, respectively.

(E) Current variation of the memory at the on and off states from the initial to 1,000 P/E cycles with an interval of 10 cycles.

(F) Retention characteristics of the memory at the on and off states with a readout voltage of V_{ds} = 0.02 V.

(G) A 2D color image of ΔI_{ds} as a function of bias voltage (x axis) and duration (y axis) in the electrical programming process.

(H) A 2D color image of ΔI_{ds} as a function of light intensity (x axis) and duration (y axis) in the optical erasing process. The device width and length were 50 and 5 μm, respectively.

back to graphene channel through the small triangular electron barrier, whereas the photogenerated holes are blocked in GDY by the large hole barrier between GDY and hBN.[6,24] These holes neutralize the residual electrons trapped in GDY film and eliminate the negative gate bias to graphene channel, making the device back to its initial state (Figure 3Div). To demonstrate that the excellent storage capability of the device is attributed to the top-floating GDY, a control experiment was performed by measuring the response of the device with a structure of Gr/hBN (without top-floating GDY) to electrical and optical stimuli. As shown in Figure S12, no obvious storage behavior has been observed in this device, indicating that GDY is essential for the memory device.

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Robust programming/erasing (P/E) endurance and ultralong retention time are essential for a nonvolatile memory. Figure 3E shows the current variation of the memory at on and off state from the initial to 10^3 P/E cycles with an interval of 10 cycles. The change of the readout currents after 10^3 P/E cycles (less than 10%) indicates a robust durability and reliability of the device. Moreover, high stability of the device is demonstrated by the long retention time over 10^5 s with less than 7% decay (Figure 3F). The robust reliability and stability of the device can be attributed to the excellent charge storage capability of GDY, as well as the top-floating-gated architecture and high hBN barrier.[19,24,37] Owing to the high DOS of GDY, the number of the trapped electrons in GDY can be tuned continuously in a wide range by adjusting the applied electrical/optical pulses, resulting in the continuous change of the channel current (Figures 3G, 3H, and S13). The controllable accumulation and release of electrons in GDY enable the optoelectronic memory to achieve multibit storage.

Multibit memory with over 256 storage levels

Multibit memories, which can store more than 1 bit data in one single device, have been regarded as an important way to increase the data storage capability in the future.[6,23–27] Generally, the number of the storage levels is one of the most key parameters for a multibit memory. Although conventional multibit memories based on 2D materials, such as MoS_2,[6,23–25] exhibits high on/off ratios larger than 10^6, the current difference between the on and off states are always less than 10^{-7} A, leading to a limited storage capability with less than 16 storage levels (4 bits). An organic optical memory with three-terminal architecture has been demonstrated to achieve 256 storage levels under light illumination.[26] However, this device requires a high operation voltage (V_g = –60 V, V_{ds} = –10 V) and features relatively small SNRs (50 for the first current level and 2.8 for the final one). In this work, the huge current difference between the on and off state (~3 μA μm^{-1} at V_{ds} = 0.02 V), as well as the ultralong retention time (>10^5 s), enable the optoelectronic memory to achieve over 256 distinct storage levels (8 bits) with large SNRs.

As shown in Figure 4A, the current increases stepwise with the number of $V_{ds\text{-}pro}$ pulses (–8 V, 1 s) in the programming process, and finally over 256 distinct storage levels (8 bits) have been achieved. Figures 4B–4D show the enlarged current steps for regions I to III in Figure 4A, which is caused by the increase of the trapped electrons in GDY triggered by each $V_{ds\text{-}pro}$ pulse. The number of the increased electrons (Δn_e) in each step was calculated in Note S2, and the results show that the electron density increases 2.3×10^{11} cm^{-2} for the first current step, and it gradually decreases to 7.3×10^{10} cm^{-2} for the final step. The SNR for current levels at the beginning exceeds 470, whereas it decreases to 150 for the final current levels, which are 2 orders of magnitude larger than that of the reported multibit memories with comparable storage levels (Note S3).[26,27]

For the optical erasing process, periodic light pulses will stepwise decrease the density of the trapped electrons in GDY film, leading to a progressive decrease of channel current with the number of pulses. As shown in Figure 4E a data storage capability of over 8 bits (256 current levels) was demonstrated by applying more than 270 periodic light pulses (450 nm, 10 mW cm^{-2}, 100 ms) with an interval of 3 s to the optoelectronic memory at V_{ds} = 0.02 V. It is worth noting that a decay of channel current is always observed on termination of optical pulses for optoelectronic floating-gate memory,[6,24,25,38] which may lead to an erroneous reading. The dynamic response of our device triggered by optical pulses has been investigated, in which a quick decay is observed on termination of optical pulse and the

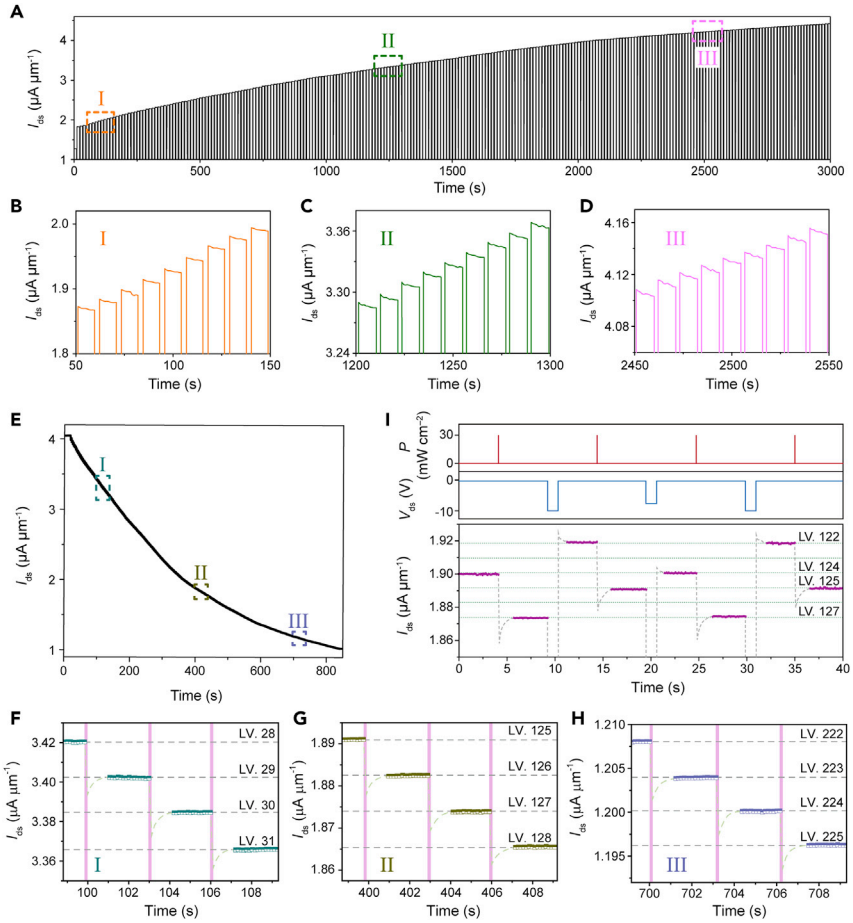

Figure 4. Multibit memory with over 256 storage levels

(A) I_{ds}-time curve of the memory under periodic $V_{ds\text{-}pro}$ pulses (–8 V, 1 s) with intervals of 10 s, showing over 256 distinct current levels.

(B–D) The enlargements of the current steps in regions I (B), II (C), and III (D), respectively, corresponding to the marked regions with the same colors in (A).

(E) I_{ds}-time curve of the memory under illumination of light pulses (450 nm, 10 mW cm^{-2}, 100 ms) with an interval of 3 s at V_{ds} = 0.02 V, demonstrating over 256 storage levels.

(F–H) The enlargements in region I (F), II (G), and III (H), respectively, which are marked in (E) with the same colors.

(I) Conductance switching of the device between different storage states.

channel conductance is saturated to a stable level after ~1 s (Figure S17). In this section, the storage levels were readout with a delay time of 1 s after each optical pulse to avoid misreading. As shown in Figures 4F–4H, stable and distinguishable storage levels have been obtained by applying optical pulses. According to the stepwise decreased current, the calculated Δn_e triggered by each optical pulse and SNRs are in the range of 3.5 × 10^{11} to 4.6 × 10^{10} cm^{-2} and 720 to 100, respectively. The switching of the multibit memory between independent storage levels has also been investigated. As shown in Figure 4I, the memory switches with a sequence of level (LV) 124, LV 127, LV 122, and LV 125 for two cycles, demonstrating the capability of the device to address independent storage levels.

As discussed above, a 7% decay of channel current is observed after 10^5 s (Figure 3F), which may lead to an erroneous reading for multibit memory after a long retention time. In our device, a CVD-grown polycrystalline hBN film was

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used as the tunneling barrier layer. The trapped charges in GDY are gradually leaked through the grain boundaries and defects of hBN film, leading to the degradation of retention characteristics. As a feasible solution, a mechanically exfoliated hBN film (~6 nm) was also used to construct GDY/hBN/Gr-based memory (Figure S18A). This device exhibits significantly improved retention characteristics, that the decay of the channel current is decreased to 2% even after 10^5 s (Figure S18B). On the other hand, a wide gap between adjacent storage levels is also important for a reliable memory. For instance, 16 storage levels with average gap of 0.2 μA μm^{-1} have been demonstrated by applying an optical pulse with higher intensity and longer duration (20 mW cm^{-2}, 1 s), exhibiting a long retention time for over 10^4 s (Figure S19).

Flexible two-terminal multibit nonvolatile memory

In conventional three-terminal floating-gate memory devices, a thick and rigid blocking oxide layer, e.g., Al_2O_3, HfO_2, and SiO_2, are always used as the dielectric and tunneling layers.[39–41] The poor bendability of these rigid blocking layers seriously limits the flexibility of the devices since frequent bending will lead to irreversible damage or even cracks to the rigid films. It has been demonstrated that devices with fully 2D-material structures exhibit considerable potentials for flexible applications owing to their 2D planer structures and ultrathin thickness. Here, the fully 2D-material-based devices with two-terminal architecture enable the development of flexible multibit memory based on GDY/hBN/Gr heterostructure.

As shown in Figures 5A and S21, a two-terminal memory device array (15 × 17) was fabricated on a flexible polyethylene terephthalate (PET) substrate using indium tin oxide (ITO) film as the source and drain electrodes. Figure 5B shows a multiple dynamic switching cycles between the on and off states by applying $V_{ds\text{-}pro}$ and light pulses for programming and erasing, respectively. The cyclic P/E endurance and retention characteristics indicate that the flexible memory exhibits robust endurance over 1,000 P/E cycles (Figure 5C) and ultralong retention time exceeding 10^5 s (Figure 5D). Moreover, the I_{ds}-time curve under periodic $V_{ds\text{-}pro}$ pulses (–10 V, 1 s) displays a stepwise increasing current (Figure 5E), indicating 64 distinct storage levels (6 bits). The SNRs of the device on PET are in the range of 300–200, indicating the potential to achieve more storage levels. In the bending test, we performed over 1,000 bending cycles to the device and measured the on and off current for every 50 bending cycles (Note S4). As shown in Figure 5F, there is no significant degradation in the on and off current even after 1,000 bending cycles, indicating a robust bending stability of the device. The excellent bending stability and reliability of the device in the bending test benefit from the two-terminal architecture and fully 2D-material structure. The two-terminal architecture without gate electrode enables the device to be constructed with fully 2D-material GDY/hBN/Gr heterostructure without thick dielectric layer. The total thickness of the device is less than 10 nm, exhibiting excellent flexibility. As illustrated in Figure S22, the strong in-plane strength and weak out-of-plane interaction (van der Waals interaction) between layers protect the GDY/hBN/Gr heterostructure against damage and cracks in the bending state. When the device returns to the flat state, the GDY/hBN/Gr heterostructure will also recover to its initial state. Therefore, the performance of the device is maintained in the bending test, demonstrating robust reliability and stability.

Conclusion

In summary, a novel EDL-confined method was developed to synthesize a few-layered GDY film with wafer scale, high crystallinity, and uniformity on copper

Please cite this article in press as: Li et al., Synthesis of wafer-scale ultrathin graphdiyne for flexible optoelectronic memory with over 256 storage levels, Chem (2021), https://doi.org/10.1016/j.chempr.2021.01.021

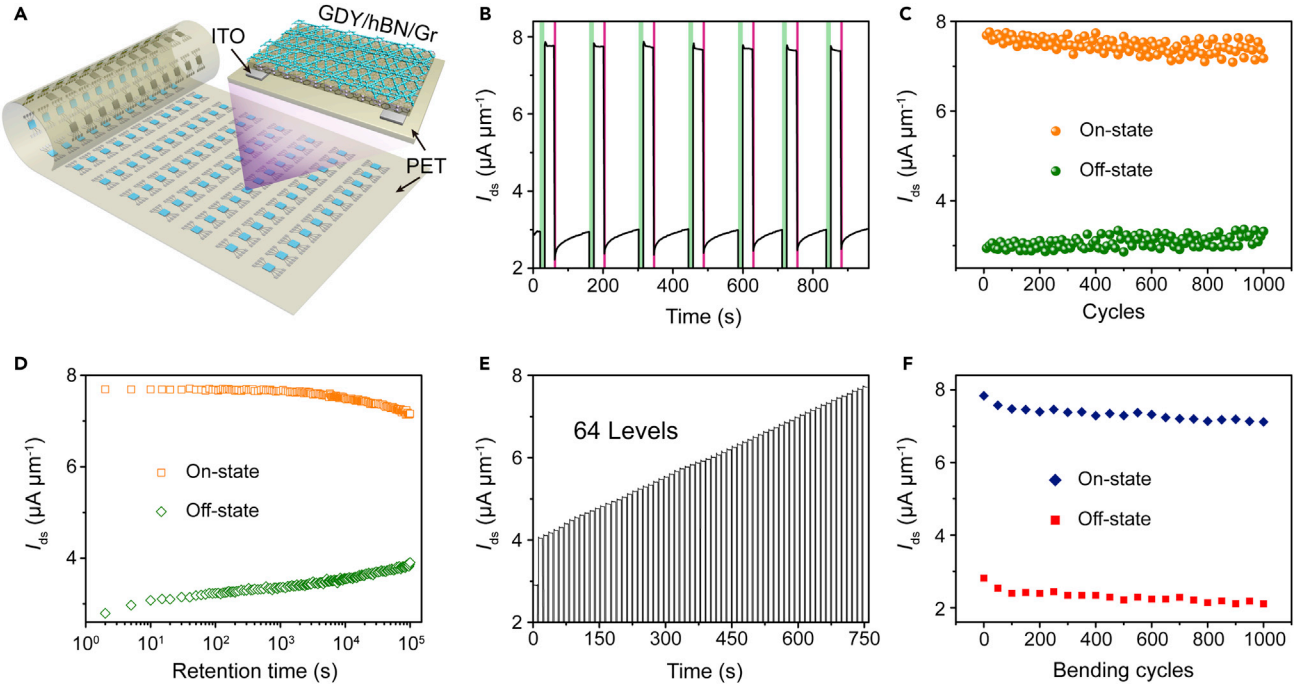

Figure 5. Two-terminal multibit nonvolatile memory on a flexible PET substrate

(A) Schematic illustration of the memory fabricated on a flexible PET substrate.

(B) Dynamic behavior of the memory in seven P/E cycles with reading voltage of V_{ds} = 0.1 V. Programming process: a $V_{ds\text{-}pro}$ pulse of –13 V for 10 s (green region); erasing process: a 450-nm light pulse with intensity of 20 mW cm^{-2} at V_{ds} = 0.1 V for 3 s (pink region).

(C) Current variation of the memory at the on and off states from the initial to 1,000 P/E cycles with an interval of 10 cycles.

(D) Retention characteristics of the memory at the on and off states with a readout voltage of V_{ds} = 0.1 V.

(E) I_{ds}-time curve of the memory under periodic $V_{ds\text{-}pro}$ pulses (–10 V, 1 s) with intervals of 10 s, showing 64 distinct current levels.

(F) Current variation of the device at the on and off states after successive bending cycles. Each cycle was performed at a bending radius of 10 mm for 5 s, followed by 5 s of waiting time. Currents were measured at V_{ds} = 0.1 V with an interval of 50 bending cycles.

foil, and a two-terminal flexible multibit optoelectronic memory based on the GDY/hBN/Gr heterostructure was investigated using GDY as a photoresponsive top-floating gate. Benefiting from the unique properties of GDY, including high DOS and WF, natural band gap, strong absorption, and 2D planar network structures, the device exhibits excellent performance including ultrahigh data storage capability (8 bits per cell) with high SNRs (>100), low operation voltage, long retention time, and robust P/E endurance. Moreover, the excellent mechanical strength and flexibility of GDY, as well as the two-terminal architecture without gate electrode and rigid blocking oxide layer, endows the device with robust bending stability (for over 1,000 bending circles). This work demonstrates the considerable potential of GDY in future flash memory and other devices, paving the way to develop GDY-based flexible optoelectronic devices in wearable systems.

EXPERIMENTAL PROCEDURES

Resource availability

Lead contact

Further information and requests for resources should be directed to and will be fulfilled by the lead contact, J.Z. (jinzhang@pku.edu.cn).

Materials availability

This study did not generate new materials.

Data and code availability

This article includes all datasets generated or analyzed in this study.

HEB preparation

To a solution of 20 mg hexakis[(trimethylsilyl)-ethynyl]benzene (HEB-TMS) and 20 mL tetrahydrofuran (THF), 0.2 mL TBAF (1 M in THF) was added under argon atmosphere and stirred at 0°C for 15 min. Then the mixture was diluted with ethyl acetate, washed two times with saturated NaCl, dried by anhydrous $MgSO_4$, and filtered. The solvent was evaporated under vacuum while maintaining the temperature below 20°C under dark. The residue was diluted in 50 mL acetone to be used as a monomer solution.

Synthesis of few-layered GDY film via EDL-confined method

GDY was synthesized with a routine two-electrode cell at room temperature. A gold foil (1 × 2 cm), a copper foil (1 × 2 cm), and 50 mL acetone were used as anode, cathode, and electrolyte, respectively. Then, 0.25- mL TMEDA and 0.2-mL monomer solutions were introduced into the cell. The voltage was set as 2 V. After reaction for 10 h at 20 °C, the cathode (copper foil) was removed from the reaction mixture and washed in turn with acetone, dimethylformamide (DMF), ethanol, and water. GDY film was obtained on copper film after drying by nitrogen flow.

Synthesis of GDY film via *in situ* Glaser coupling method

A 0.1 mL HEB solution was added to a 100-mL round-bottom flask containing acetone (50 mL), TMEDA (0.25 mL), and copper foils. The reaction mixture was kept at 20°C for 10 h. After completion of the reaction, the GDY film was grown on copper foil and washed in turn with acetone, DMF, water, and ethanol, then, dried under nitrogen flow.

Synthesis of GDY on gold foil via a control experiment

A routine two-electrode cell is introduced 50 mL acetone as electrolyte and two gold foils (1 × 2 cm) as electrodes. Then, 2-mL TMEDA containing 2 mg $Cu(OAc)_2$ and 0.2 mL HEB solution are introduced into the electrolyte in turn. The EF strength is set as 2 V. After 10 h, the cathode is removed from the reaction mixture and washed in turn with acetone, DMF, ethanol, and water. GDY film is obtained on gold film after drying by nitrogen flow.

Nonvolatile memory device fabrication and measurements

Two-terminal memory devices with the structure of GDY/hBN/Gr were fabricated on SiO_2/Si substrate and PET film, respectively. The effective channel length and width of the device on SiO_2/Si substrate were 5 and 50 μm, respectively. For the case of the device on PET film, the length and width were 10 and 65 μm, respectively. Details for the device fabrication can be found in Note S1. After the device fabrication, the electrical measurements were performed with a Keithley 4200A-SCS semiconductor parameter analyzer and a probe station in the atmosphere at room temperature.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.chempr.2021.01.021.

ACKNOWLEDGMENTS

We thank L.X. Zhong, J.L. Du, C.G. Chen, and C.W. Tan for helpful discussions. This work was financially supported by the Beijing National Laboratory for Molecular Sciences (BNLMS-CXTD-202001), the Ministry of Science and Technology of China

(2016YFA0200100 and 2018YFA0703502), the National Natural Science Foundation of China (grant nos. 52021006, 51720105003, 21790052, 51802220, and 21974004), and the Natural Science Foundation of Tianjin City (19JCYBJC17300).

AUTHOR CONTRIBUTIONS

J.Z., X.C., and J.L. designed the project. J.Z., T.L., and X.C. supervised the project. J.L. synthesized the few-layered GDY film. X.C. and Z.Z. constructed the devices and performed the electrical measurements. J.L. and X.C. performed the characterizations and wrote the manuscript. All authors discussed the results and contributed to the interpretation of data and contributed to editing the manuscript.

DECLARATION OF INTERESTS

The authors declare no competing interests.

Received: August 7, 2020
Revised: November 16, 2020
Accepted: January 26, 2021
Published: February 26, 2021

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