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Substrate Engineering by Hexagonal Boron Nitride/SiO_2 for Hysteresis-Free Graphene FETs and Large-Scale Graphene p–n Junctions**

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Abstract: We have explored an approach for the fabrication of intrinsic and hysteresis-free graphene field-effect transistors (FETs) and for the construction of graphene p–n junctions based on substrate engineering by hexagonal boron nitride (h-BN)/SiO_2. The effect of various interfaces on the performance of the graphene FETs was systematically studied by constructing four types of graphene devices (graphene/SiO_2 FETs, graphene/h-BN FETs, h-BN/graphene/SiO_2 FETs, and h-BN/graphene/h-BN FETs). Graphene/SiO_2 FETs and h-BN/graphene/SiO_2 FETs always exhibit large hysteresis before and after annealing, whereas graphene/h-BN FETs and h-BN/graphene/h-BN FETs show intrinsic properties after annealing. Raman measurements also indicate that graphene on a SiO_2 substrate contains large amounts of p-doping, whereas that on a h-BN substrate is intrinsic. Thus, the graphene/h-BN interface gives intrinsic and hysteresis-free graphene FETs, whilst the graphene/SiO_2 interface affords p-doping and a hysteresis effect in the graphene FETs. This result is because h-BN serves as an insulation layer, which prevents charge trapping between the graphene and the charge traps at the graphene/SiO_2 interface, which cause the hysteresis. In addition, the negligible electrostatic doping of h-BN into graphene also ensures the intrinsic and hysteresis-free properties of graphene/BN/SiO_2 FETs. Moreover, benefitting from the p-doped and intrinsic features of graphene on SiO_2 and h-BN substrates, respectively, large-scale graphene p–n junction superlattices with great potential difference are constructed and integrated into photodetector arrays by substrate engineering with h-BN/SiO_2. Efficient hot carrier-assisted photocurrent was generated by laser excitation at the junction under ambient conditions.

Keywords: boron nitride · hysteresis · field-effect transistors · graphene · substrate engineering

Introduction

Since its discovery in 2004,[1] graphene has been considered to be the most-promising candidate for next-generation electronic devices, owing to its superior electrical properties and unique 2D structure.[2] Graphene-based field-effect transistors (FETs) show exceptional carrier density and polarity tunability, high current densities, as well as extraordinarily high mobility for both electrons and holes.[3] However, the nature of graphene, a one-atom thick carbon membrane in which every atom is exposed to the external environment, makes it highly sensitive towards its local surroundings, such as substrate curvature[4] and charge traps at interfaces.[5,6] This high sensitivity causes the graphene-based FETs to exhibit low carrier mobility, heavy doping, and, in particular, a large hysteresis effect when measured under ambient conditions.[7–9] In particular, the field-effect properties show dependence on the measurement parameters and environmental variation, which hampers the accurate assessment of the performance of graphene FETs.[7,10,11] In spite of some efforts towards the development of more intrinsic and high-carrier-mobility graphene FETs,[3,12,13] several challenges remain. For example, the preparation of suspended graphene devices requires a number of complex fabrication steps and is usually expensive, which is unsuitable for large-scale technological applications. Moreover, modifying the substrate with organic molecules is limited by the stability of molecules and vacuum annealing is difficult to perform experimentally; thus, an even-larger p-doping and hysteresis effect will arise after re-exposing the device to ambient air.[4,10,13] Therefore, it is critical to develop an effective and reliable method for suppressing the doping and hysteresis effects for the future application of graphene FETs.

According to a previous study, the charge trapping/detrapping between graphene and charge traps at a graphene/SiO_2 interface causes the doping and hysteresis effects in graphene FETs.[9,10,14] Thus, the introduction of a stable insulation layer that can suppress such charge trapping/detrapping

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[**] FET = Field-effect transistor.

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should be an effective way of suppressing the hysteresis effect. Hexagonal boron nitride (h-BN) is a promising material as a substrate for graphene devices, because of its hydrophobicity, atomically smooth surface, large electrical band-gap, low dielectric constant (about 4), chemical inertness, etc.[3,15] As such, the combination of graphene and h-BN has attracted great attention because it has potential to open up the exciting possibility of creating a new class of graphene-based electronic devices.[16–18] Previous work has shown that the mobility and the local electronic properties of graphene can be greatly improved when deposited onto a h-BN substrate, owing to its ultra-flat surface.[15,17] h-BN has also been used as a dielectric layer for graphene devices.[19] In addition, theory predicts that a band-gap can be opened up in graphene if it is sandwiched between two h-BN films.[20] In particular, h-BN can be used as a barrier layer in BN/graphene/BN multilayered heterostructures for electron tunneling between two graphene layers and for graphene-based vertical tunneling transistors.[18] So, to reveal whether electrostatic doping exists at the graphene/BN interface, it is also critical to study combined graphene and h-BN electronic devices.

Herein, we have systematically studied the effect of different interfaces (graphene/SiO_2, graphene/h-BN/SiO_2, h-BN/graphene/SiO_2, and h-BN/graphene/h-BN) on the performance of graphene FETs to explore the way of suppressing the doping and hysteresis in graphene FETs (Figure 1). Electrical and Raman properties show that the graphene/SiO_2 interface introduces p-doping and hysteresis effects into graphene FETs, whilst the graphene/BN interface gives intrinsic and hysteresis-free graphene FETs. These results indicate that charge trapping/detrapping of graphene with charge traps from the graphene/SiO_2 interface, which cause the hysteresis, can be effectively blocked by insulating with a h-BN layer. Furthermore, a large-scale and periodic graphene p–n junction was constructed through BN/SiO_2 substrate engineering, which is beneficial for the integration of large-scale graphene-based optoelectronic devices for future applications.

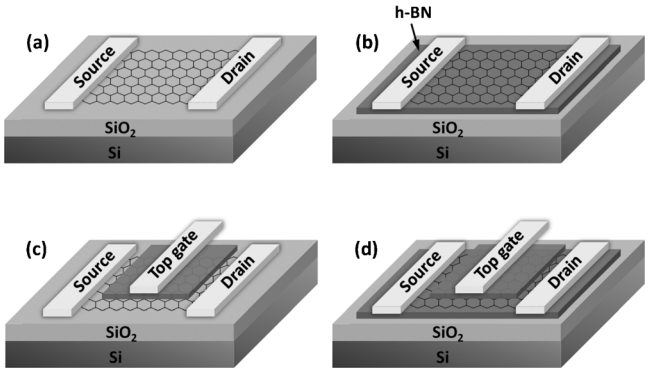

Figure 1. Schematic representation of four types of graphene FETs: a) Graphene on a SiO_2 substrate forms typical graphene/SiO_2 FETs; b) graphene on a h-BN substrate forms graphene/BN/SiO_2 FETs; c) graphene sandwiched between SiO_2 and h-BN substrates forms BN/graphene/SiO_2 FETs; and d) graphene sandwiched between two h-BN substrates forms BN/graphene/BN FETs.

Results and Discussion

First, we focused on the electrical field-effect properties of graphene/SiO_2 FETs (that is, a graphene-based device that was fabricated on a SiO_2 substrate). Figure 2a shows a plot

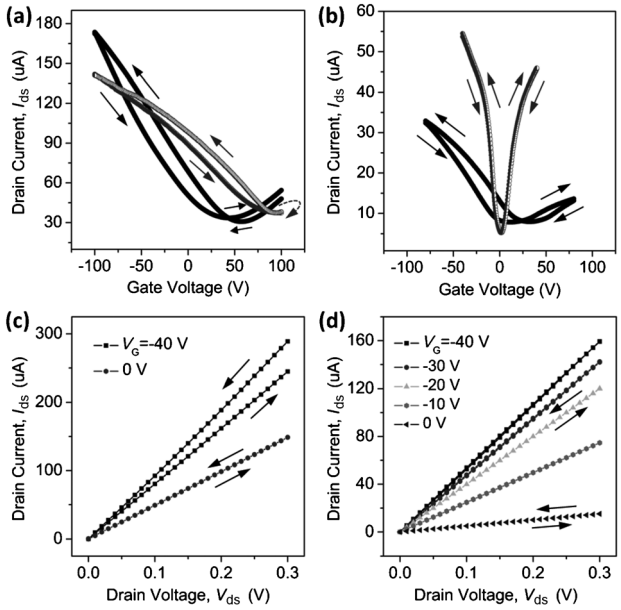

Figure 2. Representative transfer curves of a) graphene/SiO_2 FETs and b) graphene/BN/SiO_2 FETs before (black) and after annealing (gray). The back-gate voltage, V_{B-G}, is swept from -100 V to $+100$ V and then back to -100 V at a rate of 0.1 V s^{-1}. Output curves of c) graphene/SiO_2 FETs and d) graphene/BN/SiO_2 FETs after annealing. The drain voltage, V_{ds}, is reversibly swept from 0 V to 0.3 V under different V_{B-G} values. The arrows in (a,b) and (c,d) denote the directions of the V_{B-G} and V_{ds} sweeps, respectively.

of the source-drain current (I_{ds}) as a function of the reverse back-gate voltage (V_{B-G}) that was applied to the silicon back gate of the graphene/SiO_2 FETs before and after annealing in a H_2/Ar flow at 350 °C for 3 h. The transfer curves that were recorded during the up and down sweeps of V_{B-G} of graphene before annealing showed poor reproducibility and each curve showed asymmetry between the electron and hole doping. The gate voltage that corresponded to the charge-neutral point (V_{Dirac}) for these two curves showed a large splitting ($\Delta V_{Dirac} = 30$ V). In addition, the output curves of graphene/SiO_2 FETs with V_{ds} reversible sweeping between 0 V and 0.3 V showed very good reversibility at $V_{B-G} = 0$ V, whereas they showed clear splitting at $V_{B-G} > 0$ V, as shown in Figure 2c. All of these phenomena indicate that the graphene device that is fabricated on a SiO_2 substrate has large p-doping and hysteresis effects. The origin of the p-doping and the gate hysteresis in graphene/SiO_2 FETs, which has long been studied but remains disputed, is

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usually attributed to the charge trapping of graphene by the charge traps of H_2O/O_2 molecules,[4,9,10] the SiO_2 dielectric layer,[5] photoresist residues, or other contaminants.[13] Furthermore, heavy p-doping and a large gate hysteresis arise in graphene/SiO_2 FETs after annealing and the V_{Dirac} for these two curves shifts to more-positive values such that are even outside of our V_{B-G} sweep range. This phenomenon is usually observed in traditional graphene/SiO_2 FETs, although the reason for it is still debated. The carrier mobility was calculated from the linear regime of the transfer characteristics according to Equation (1), where C_g is the gate capacitance of the dielectric materials, I_{ds} is the drain current, V_G is the gate voltage, and μ_{FET} is the field-effect mobility.[5]

$$\mu_{FET} = \frac{L}{C_g W V_d} \frac{dI_d}{dV_G} = g_m \frac{L}{V_d W C_g} \quad (1)$$

dI_d/dV_G was calculated from the slope to be between $V_G = -40$ V and V_{Dirac}. The calculated hole-carrier mobility (μ) of graphene/SiO_2 FETs was only 5740 $cm^2V^{-1}s^{-1}$ at $V_{ds} = 0.1$ V; this low mobility is attributed to doping-induced scattering of the transport carriers in graphene.

In contrast, the electrical field-effect properties of graphene/BN FETs (that is, a graphene device that was fabricated on a h-BN substrate) were very different to those of graphene/SiO_2 FETs, as shown in Figure 2b. The transfer curves for graphene/BN/SiO_2 FETs before annealing exhibited relatively small p-doping and gate hysteresis ($\Delta V_{Dirac} = 30$ V), owing to the charge trapping/detrapping of graphene with charge traps (H_2O/O_2, residues, or others) that were introduced during the transfer process. However, the transfer curves under V_{B-G} up and down sweeping showed extremely good reproducibility and the V_{Dirac} of these two curves hardly changed (about 0 V) after annealing the device to remove the charge traps. The suppression of the hysteresis effect in graphene/h-BN FETs is also reflected in their output properties, as shown in Figure 2d; the output curves with V_{ds} reversible sweeping between 0 V and 0.3 V show very good reversibility at all V_{B-G} values. In particular, the carrier mobility of the graphene/BN/SiO_2 FETs is greatly increased (28630 $cm^2V^{-1}s^{-1}$ at $V_{ds} = 0.1$ V), owing to the suppression of doping-induced scattering in graphene. Moreover, the electrical field-effect properties of graphene/h-BN FETs exhibit much-higher stability compared to graphene/SiO_2 FETs, as shown in the Supporting Information, Figure S3. Herein, we have to emphasize that the two strict annealing processes, that is, annealing h-BN in air after being cleaved onto a SiO_2 substrate and annealing the graphene/h-BN complex after transfer, are very important for decreasing the contact resistance and increasing the carriers mobility of these devices, as shown in the Supporting Information, Figure S4.

To further clarify the effect of different interfaces on the properties of graphene FETs, we studied the field-effect properties of h-BN/graphene/SiO_2 FETs and h-BN/graphene/h-BN FETs. For h-BN/graphene/SiO_2 FETs, graphene/BN and graphene/SiO_2 interfaces were formed on the top and bottom surfaces of graphene, receptively. As with graphene/SiO_2 FETs, the transfer curves of h-BN/graphene/SiO_2 FETs at the bottom gate exhibited large p-doping and gate hysteresis, as shown in Figure 3a. This result should be

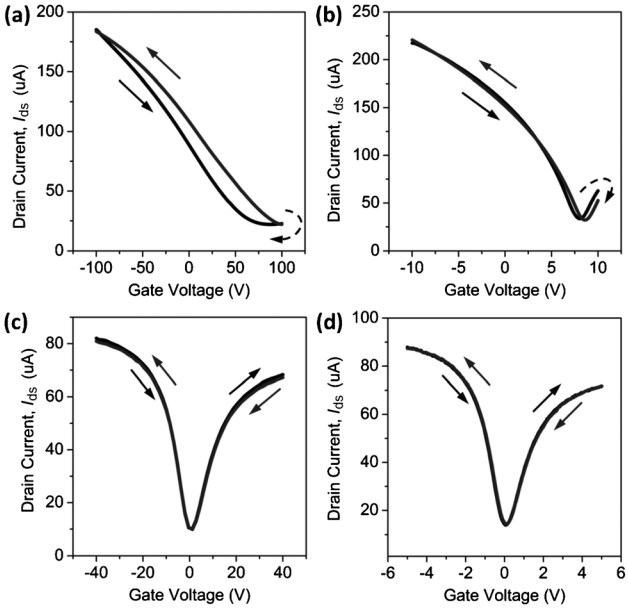

Figure 3. Representative transfer curves of BN/graphene/SiO_2 FETs under reversible a) bottom-gate (V_{B-G} from −100 V to +100 V) and b) top-gate sweeping (V_{T-G} from −10 V to 10 V). Transfer curves of BN/graphene/BN FETs under reversible c) bottom-gate (V_{B-G} from −40 V to +40 V) and d) top-gate sweeping (V_{T-G} from −4 V to +4 V). $V_{ds} = 0.1$ V. The arrows in these figures denote the sweep direction of the gate voltage. Both BN/graphene/SiO_2 FETs and BN/graphene/BN FETs were annealed at 350 °C for 2 h to remove the residues device fabrication before the electrical measurements.

due to the charge trapping/detrapping of graphene with charge traps from both dielectric SiO_2 and H_2O/O_2 at the graphene/SiO_2 interface. Moreover, the transfer curves of this device at the top gate, with h-BN as a dielectric layer, also exhibited p-doping and hysteresis (Figure 3b). This result shows that the H_2O/O_2 charge traps, which only exist at the graphene/SiO_2 interface, still cause the gate hysteresis in this top-gate device, because there is no electrostatic charge transfer at the graphene/h-BN interface (see below). Thus, just protecting the top surface with h-BN cannot suppress the doping and gate hysteresis because the charge traps come from the graphene/SiO_2 interface, rather than the graphene/air interface. For BN/graphene/BN FETs, two graphene/h-BN interfaces were formed on the top and bottom surfaces of graphene. As shown in Figure 3c,d, the p-doping and gate hysteresis were effectively suppressed at both the top and bottom gates, which indicates that there is no electrostatic charge transfer at the graphene/h-BN interface. This result is important for the use of h-BN as a dielectric or barrier layer for combined graphene and h-BN electronic devices.

From this above study of the effect of different interfaces on the performance of graphene FETs, we know that the

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charge traps that cause p-doping and gate hysteresis in graphene/SiO_2 FETs mainly come from the graphene/SiO_2 interface. The introduction of a thin hydrophobic layer of h-BN as insulation between graphene and the SiO_2 substrate can block the charge trapping and, thus, suppress the p-doping and gate hysteresis. That is, for high-performance graphene FETs, there is the good (the h-BN substrate), the bad (the SiO_2 substrate), and the ugly (charge traps from the graphene/SiO_2 interface). However, this difference between graphene on h-BN and SiO_2 substrates is beneficial for constructing graphene heterojunctions.

Graphene heterojunctions are attracting great interest, owing to their potential use in the field of high-speed photodetectors,[21] photovoltaics, and thermoelectricity.[22] More recently, it has been shown that a graphene superlattice structure can lead to a number of fascinating new phenomena, including electron-beam supercollimation, anisotropic transmission, the creation of additional Dirac cones, and effective magnetic fields.[23] To date, most graphene heterojunctions have been fabricated by using multiple electrostatic gates,[24] electrical stress-induced doping,[25] chemical treatment by gas exposure,[10] chemical modifications on the top of graphene,[26] and modification of the substrate by self-assembled monolayers.[27] However, current methods for electrostatic gating require a number of fabrication steps, which may not be easily scalable on an industrial level and are usually expensive. Furthermore, chemical doping on the top of graphene can degrade the carrier mobility in the device through the introduction of defects and impurities into the graphene. In addition, physisorbed dopant molecules are not stable and may be desorbed, which would result in changes in the electronic properties of graphene. Thus, the development of a facile and scalable technique for the construction of graphene heterojunctions is needed.

From these above results, we know that h-BN and SiO_2 substrates afford intrinsic and p-doped graphene, respectively. Thus, there should be a potential difference between graphene on h-BN and SiO_2 substrates when a graphene sheet is stretched across these two substrates, as shown in Figure 4a. Figure 4b shows an optical image and Raman features of graphene that has been deposited across h-BN and SiO_2 substrates; the dashed square denotes the area that was scanned for Raman imaging. The Raman mapping of the G-band frequency (ω_G), the 2D-band frequency (ω_{2D}), and the intensity ratio of the 2D (I_{2D}) and G bands (I_G), I_{2D}/I_G, which can be used to judge the doping of graphene,[28] is shown in Figure 4b. This mapping reveals a remarkable ω_G shift from about 1585 cm^{-1} in the h-BN substrate area (middle section) to about 1595 cm^{-1} in the SiO_2 substrate area (right section), thereby clearly indicating two distinct surfaces. In addition to an up-shift in ω_G ($\Delta\omega_G \approx 10\ cm^{-1}$), an up-shift in ω_{2D} ($\Delta\omega_{2D} \approx 10\ cm^{-1}$) and a decrease in I_{2D}/I_G on moving from the from h-BN area to the SiO_2 area are also seen. For a clearer comparison, the typical Raman spectra for the two spots on the graphene in the SiO_2 and h-BN regions are shown in Figure 4b, top right. The Raman spectrum of graphene on the SiO_2 substrate (right section) exhibits a typical p-doping effect on the spectroscopic characteristics of the G and 2D bands, whilst that on the h-BN substrate (middle section) not only shows typical spectroscopic characteristics of intrinsic graphene, but also an additional peak at 1367 cm^{-1}, which is ascribed to the Raman signals of the underlying h-BN film. Thus, the observed up-shifts in ω_G and ω_{2D} and the decrease in I_{2D}/I_G of graphene on moving from the BN substrate region to the SiO_2 substrate region, which are attributed to the p-doping of graphene, indicate that a graphene p–n junction is formed at the boundary of the SiO_2 and h-BN substrates. (In fact, it should be more accurately defined as a p–i junction, but herein we call it a p–n junction because it is homogeneously formed in the same graphene film.) The potential difference of the graphene p–n junction, $\Delta E_F = |E_{F(SiO2)} - E_{F(BN)}|$, can be approximately calculated from the shift in the G-band frequency, $\Delta\omega_G = |\omega_{G(SiO2)} - \omega_{G(BN)}|$, according to Equation (2), where $\langle D_\Gamma^2 \rangle_F = 45.6\ eV^2\ Å^{-2}$ is the deformation potential of the E_{2g} mode, M is the atomic weight of carbon, ω_0 is the frequency of the G band in undoped graphene, v_F is the Fermi velocity of graphene, and $\alpha' = 4.39 \times 10^{-3}$.[29]

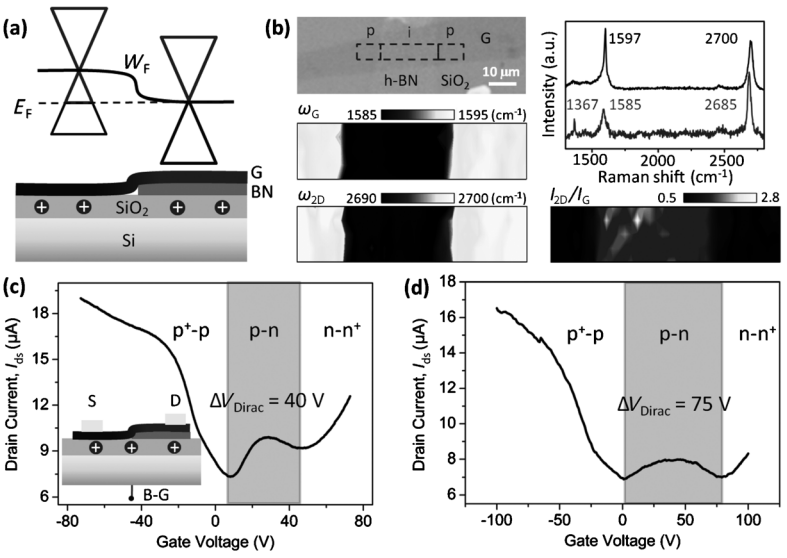

Figure 4. a) Schematic representation of the potential profile of a graphene p–n junction that was constructed by BN/SiO_2 substrate engineering. b) Raman spectra and imaging of graphene that was stretched across BN and SiO_2 substrates. Transfer curves of graphene that was stretched across the h-BN and SiO_2 substrates c) before and d) after annealing.

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$$\hbar\Delta\omega = \frac{\hbar A\langle D_T^2\rangle_F}{\pi M\omega_0(\hbar v_F)^2}|\in_F| = \alpha'|\Delta E_F| \quad (2)$$

The corresponding carrier density can be expressed by $\Delta n = \pi^{-1}(E_F/\hbar v_F)^2$ ($\hbar v_F \approx 5\,e$ Å). For a graphene p–n junction, $\Delta\omega_G \approx 10\,cm^{-1}$, as calculated from the difference between the observed $\omega_{G(SiO2)} = 1595\,cm^{-1}$ and $\omega_{G(BN)} = 1585\,cm^{-1}$, thus signifying a potential difference of $\Delta E_F \approx 0.250$ eV, which corresponds to a hole-carrier density of $\Delta n \approx 1.25\times10^{13}\,cm^{-2}$.

To investigate the electrical transport properties of this graphene p–n junction, we prepared a device in which the graphene channel was stretched across h-BN and SiO_2 substrates. Figure 4c shows a transfer curve of FETs with a graphene p–n junction before annealing. We observed two different V_{Dirac} points, at $V_{B-G} \approx 8$ V and $V_{B-G} \approx 48$ V, which corresponded to the V_{Dirac} of graphene on h-BN and SiO_2 substrates, respectively. On the basis of the two separated V_{Dirac}, three distinct regions in the I_{ds}–V_G graph of the graphene p–n junction FETs can be identified as p^+–p, p–n, and n–n^+ regions. Graphene on both SiO_2 and h-BN substrates are p-doped at $V_{B-G} < 8$ V. Graphene on a SiO_2 substrate is p-doped, whereas graphene on a h-BN substrate is n-doped within the range $V_{B-G} = 8$–48 V. Graphene on both SiO_2 and h-BN substrates are n-doped at $V_{B-G} > 48$ V. The potential difference between the Dirac points, as revealed by the double V_{Dirac}, clearly confirms the existence of a graphene p–n junction. The potential difference of a graphene p–n junction can also be approximately calculated from $\Delta V_{Dirac} = |V_{Dirac(SiO2)} - V_{Dirac(BN)}|$, according to Equations (3) and (4),where $v_F = 10^6\,m\,s^{-1}$, n, C_a, e, and V_{Dirac} are the Fermi velocity, charge density, gate capacitance, electron charge, and the gate voltage that corresponds to the charge-neutral Dirac point, respectively.[30]

$$E_F(n) = -\mathrm{sgn}(n)\hbar v_F\sqrt{(\pi|n|)} \quad (3)$$

$$n = \alpha V_g = C_g(V_g - V_{Dirac})/e \quad (4)$$

For the graphene p–n junction before annealing, $\Delta V_{Dirac} = |V_{Dirac(BN)} - V_{Dirac(SiO2)}| \approx 40$ V and the potential difference is $\Delta E_F \approx 0.196$ eV. Furthermore, after annealing the graphene p–n junction FETs, the $V_{Dirac(BN)}$ negatively shifts to about 0 V, whilst $V_{Dirac(SiO2)}$ positively shifts to about 75 V. These results correspond to our results in Figure 2a,b, that is, that thermal annealing makes graphene on h-BN substrate more intrinsic, whilst it causes a large p-doping of graphene on a SiO_2 substrate. The value of ΔV_{Dirac} increases to about 75 V, thus signifying a potential difference of $\Delta E_F \approx 0.268$ eV, which matches well with the value that was calculated from ω_G ($\Delta E_F \approx 0.250$ eV).

The remarkably large ΔE_F value of our graphene p–n junction facilitates the efficient generation of a photocurrent under illumination, based on the photothermoelectric (PTE) effect, as shown in Figure 5a. As a demonstration, one graphene p–n junction that had been constructed by substrate engineering with h-BN/SiO_2 was embedded into a two-terminal device (Figure 5b, inset). A focused 632.8 nm laser spot (diameter ≈ 2 μm, about 1 mW) was used to excite the photocarriers. As shown in Figure 4b, the p–n junction produced a pronounced current shift when illuminated by the laser, thus indicating its capability of photoelectric conversion. The photocurrent can be reversibly switched between "ON" and "OFF" states under dark and photo-illumination (Figure 5c). Thus, the reliability and stability of the photodetector were confirmed. We further conducted photocurrent mapping of the device (Figure 5d) and clearly observed that the photocurrent was generated over the junction, as well as the two electrodes, in contrary directions. Moreover, the intensity of the photocurrent that was generated at the junction (about 40 nA) was much higher than that at the graphene/electrodes junctions (about 4 nA), thus indicating a higher efficiency for potential photodetector applications. The gate-dependent photocurrent at the channel of the p–n junction device is significantly different to that at a source-and-drain electrode (see the Supporting Information, Figure S4), which is consistent with photocurrent generation based on the PTE effect. Basis on this above analysis, the photocurrent response of a graphene p–n junction can be greatly improved by thermally annealing the device to enlarge the ΔE_F. A photocurrent response of up to $0.125\,mA\,W^{-1}$ can be obtained for a device with a graphene p–i junction that was constructed by substrate engineering with h-BN/SiO_2 substrates after annealing at 350 °C for 3 h (see the Supporting Information, Figure S5).

In addition to the advantage of easier preparation, another advantage of the construction of graphene p–n junctions by substrate engineering with BN/SiO_2 is its scalable production. Benefitting from recent progress in the chemical vapor deposition (CVD)-based growth of large-area graphene and h-BN films,[31] large-scale and periodic graphene p–n junctions of various morphologies can be constructed by substrate engineering with h-BN/SiO_2 (see the Supporting Information, Figures S6 and S7). Thus, we further studied the integration of multiple graphene photodetector channels (Figure 5e) by integrating the p–n junction superlattices into graphene photodetector arrays. A laser spot with a diameter of about 5 μm was shone over three p–n junction channels to produce photocarriers. On sweeping the laser spot from points (i) to (vi), we observed six terraces in the photocurrent–time plot, which corresponded to the positioning of the laser spot over single, double, and triple p–n junction channels. Photocurrent signals from individual channels, as well as their additions, are shown in Figure 5f. Clearly, the photocurrent multiplied with the increasing number of p–n junction channels, thus confirming the possibility of forming integrated photodetector arrays based on substrate engineering with h-BN/SiO_2 for potential applications in photovoltaic and multiple-signal computing.

Conclusions

In summary, we have systematically studied graphene/substrate interfaces for enhancing the performance of gra-

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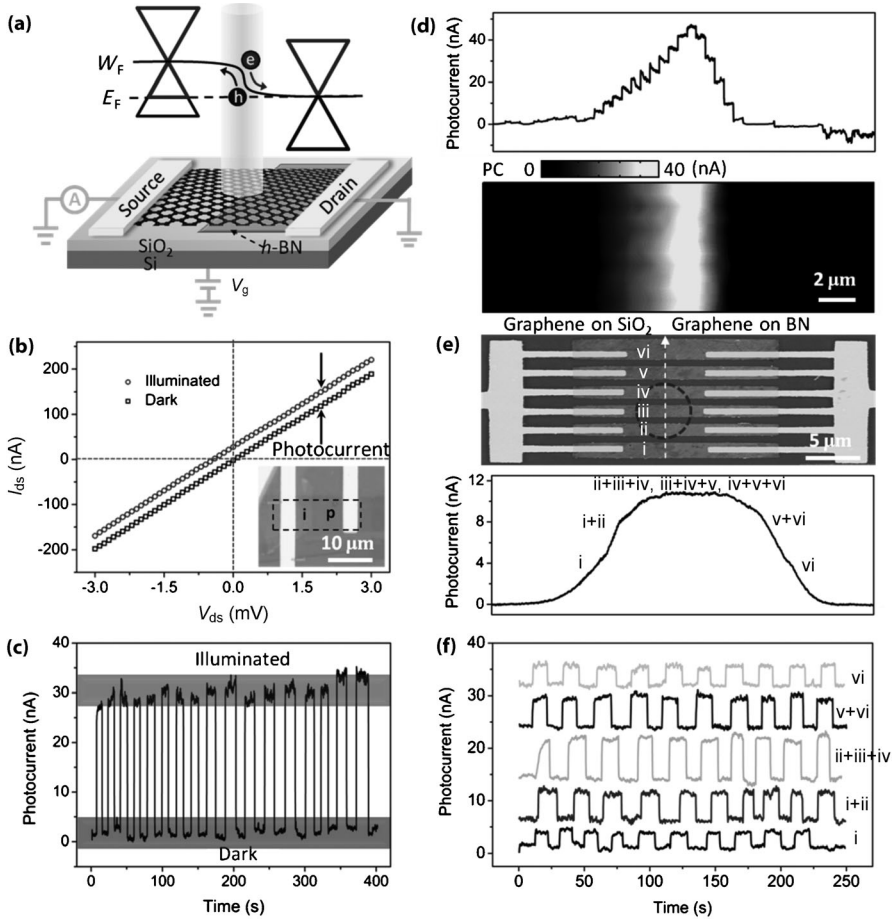

Figure 5. a) Schematic representation of the photocurrent generation of a graphene p–n junction that was constructed by BN/SiO_2 substrate engineering. b) Plot of current versus source-drain bias with (circles) and without a 632.8 nm laser beam (squares) that was focused on the p–n junction. The difference between the two curves represents the photocurrent. Inset shows the OM image of the device. c) Photoelectric response and d) photocurrent mapping (top: line mapping, bottom: area mapping) of the graphene p–n junction that was constructed by BN/SiO_2 substrate engineering. e) Top: False-colored SEM image of integrated graphene p–n photodetector arrays. Individual channels are labeled from i–vi, with sharing of the source and drain electrodes. The dashed circle represents the size and position of the laser spot. Bottom: Photocurrent line-mapping from i–vi. f) Photoelectric response of individual channels and their additions.

phene-based FETs by using substrate engineering with h-BN/SiO_2. The h-BN/graphene interface gives intrinsic, hysteresis-free, and high-mobility graphene FETs, because there is no electrostatic charge trapping at the graphene/BN interface; in particular, the h-BN film can suppress the charge trapping at the graphene/SiO_2 interface, which causes the poor performance of graphene/SiO_2 FETs. The absence of charge trapping at the graphene/BN interface affords the opportunity for the fabrication of high-performance graphene FETs and more-complex BN/graphene/BN sandwich-structured electronic devices. Finally, by using the p-doping effect of graphene on a SiO_2 substrate and the intrinsic features of graphene on a h-BN substrate, we constructed large-scale and periodic graphene p–n junctions by depositing graphene onto a patterned h-BN/SiO_2 substrate. The p–n junctions between two portions can be used for efficient photocurrent generation through the photothermoelectric effect. This approach provides an effective way to construct graphene-based superlattices with well-controlled widths and structures for future applications, such as in optoelectronic devices and electron-beam supercollimation.

Experimental Section

Fabrication of Four Types of Graphene FETs

Graphene was prepared by the mechanical exfoliation of Kish graphite onto a Si wafer that was coated with an oxide layer (SiO_2, 300 nm); the formation of monolayer graphene was identified by optical microscopy (OM) and Raman spectroscopy. Relatively thick (10–30 nm) hexagonal-BN (h-BN) flakes were cleaved onto another substrate and then annealed at 500 °C in air for 3 h to remove any residues. Optical imaging, Raman spectroscopy, and atomic force microscopy (AFM) showed that high-quality and ultra-flat h-BN flakes of various thickness had been obtained (see the Supporting Information, Figure S1). Graphene/SiO_2 FETs were prepared by using standard electron-beam lithography and lift-off techniques, as described in our previous work.[10] The electrodes were made of Cr/Au (5 nm:50 nm). Graphene/h-BN/SiO_2 FETs were fabricated by using the following multistep procedure: First, a graphene flake was transferred onto the top of a h-BN flake by using the position-selective transfer technique. Second, the graphene/h-BN/SiO_2 complex was annealed at 350 °C for 3 h to remove the residues that were formed during the transfer process. Third, standard electron-beam lithography and lift-off techniques were used to fabricate the contact electrodes onto the graphene. h-BN graphene/SiO_2 FETs and h-BN/graphene/h-BN FETs were fabricated by using similar methods, but with a few differences. For h-BN/graphene/SiO_2 FETs, a h-BN flake was transferred onto the top of graphene on the SiO_2 substrate. For h-BN/graphene/h-BN FETs, two-step position-selective transfer was used: First, a graphene flake was transferred onto the top of a h-BN flake to form the graphene/BN structure; then, another h-BN flake was transferred onto the top of the graphene/BN complex to form the BN/graphene/BN sandwich structure. Besides the general bottom-gated graphene FETs, top-gated graphene FETs, with h-BN as the dielectric layer, were also constructed in the same device by adding a contact electrode onto the h-BN layer. The OM image of these four types graphene devices are shown in the Supporting Information, Figure S2. All of these samples were annealed under a H_2/Ar atmosphere at 350 °C for 3 h after each transfer step, which was critical for improving the performance of graphene FETs, as discussed below.

Substrate Engineering Construct Graphene p–n Junction

Graphene was stretched across the BN and SiO_2 substrates by using the position-selective transfer technique. The source and drain electrodes were contacted onto the graphene on the BN and SiO_2 substrates, respec-

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tively, which made the graphene channel stretch across the BN and SiO_2 substrates.

Raman, Electrical, and Photoelectrical Measurements

Raman spectra were recorded on a Horiba HR800 Raman system with a 514.5 nm laser at a grating of 600 lines mm^{-1}. The incident laser beam was focused by a 100× objective and the laser power on the samples was kept below 0.5 mW to avoid laser-induced heating. Electrical measurements were performed on a Keithley 4200 semiconductor analyzer. All of the measurements were performed at RT in ambient air.

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