ADVANCED MATERIALS

Towards Entire-Carbon-Nanotube Circuits: The Fabrication of Single-Walled-Carbon-Nanotube Field-Effect Transistors with Local Multiwalled-Carbon-Nanotube Interconnects

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With scaling down of electronics occurring according to Moore's law, channel doping and problems with interconnects are becoming more challenging for the current and next-generation silicon complementary metal oxide–semiconductor (CMOS) technology.[1] In Si-based CMOS devices, the polarity of the device, that is, whether the channel is p- or n-type, is defined by doping. As devices are becoming smaller, the channel doping has to increase significantly to overcome short-channel effects and to properly set the threshold voltage. However, high channel doping reduces carrier mobility and increases leakage power consumption. Moreover, the total number of dopants in the channel of an extremely small MOS field-effect transistor (FET) will be reduced to several hundred or even less. The statistical fluctuation in the number and location of the dopants will increase rapidly as the device size is reduced, resulting in sharply increased variability of the threshold voltage from device to device, rendering circuit design an even more difficult job. In addition to the above-mentioned problems with MOSFETs, the reduced interconnects also suffer from increasing current density.[1] As the device size shrinks, electron scattering from grain boundaries and interfaces increases, which in turn increases the effective resistivity of the currently used copper interconnects. This increasing resistivity as well as the rising current density may eventually lead to an electromigration failure of the Cu interconnects.

Extensive investigations have been carried out to search for alternatives for both CMOS-fabrication technologies and interconnect materials. Carbon nanotubes (CNTs), because of their novel structures and properties, have been regarded as one of the most promising building blocks for future integrated circuits.[2,3] Depending on its helicity, a CNT can be either semiconducting or metallic. While a semiconducting CNT can be used for fabricating FETs, a metallic one may be utilized in interconnects.[4] In principle, a CMOS circuit based entirely on CNTs may therefore be fabricated. However, no such prototype device has been reported until now.

In a recent paper,[5] we showed that doping can be completely avoided in the processes used to fabricate CNT-based CMOS circuits. With this doping-free technology, a CMOS inverter, which is the basic unit in large-scale integrated circuits, can be readily fabricated by simply depositing two Pd and two Sc contacts onto a single semiconducting CNT. Since this technology does not require doping, the problem associated with the threshold-voltage variation caused by a statistical fluctuation in the number of dopants in the conduction channel is avoided. Furthermore, because of the 1D nature of CNTs, the electron mean-free-path in metallic CNTs can be very large, typically up to a few micrometers.[4,6] The strong C–C bonds in the CNT also lead to extraordinary mechanical strength and a very large current-carrying capacity of up to $10^9\,A\,cm^{-2}$ (about 1000 times larger than that of Cu).[7,8] In addition, the high thermal conductivity[9] and inert surface of the CNTs also render them compatible with Si CMOS technology. Therefore, CNTs provide a highly promising solution for improving the performance of present interconnects in terms of speed, power dissipation, and reliability.

It has been suggested that metallic single-walled CNTs (SWCNTs) or multiwalled CNTs (MWCNTs) may be used to replace Cu interconnects, and the idea has been explored by many research groups.[8,10–17] CNTs have been integrated into silicon CMOS circuits for use as both higher-level interconnects and vertical vias.[10–12,14,15] In particular, it was recently demonstrated that such CNT-interconnected silicon integrated circuits can be operated above 1 GHz.[17] It is now well-established that CNT-based p- and n-type CNT FETs may significantly outperform state-of-the-art Si-based MOSFETs.[18–23] However, direct integration of SWCNT FETs with CNT interconnects has not yet been reported. In this study, SWCNT FETs in which MWCNTs are used as local interconnects are fabricated and shown to work well, making a successful first step towards CMOS circuits fabricated entirely from carbon.

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DOI: 10.1002/adma.200802758

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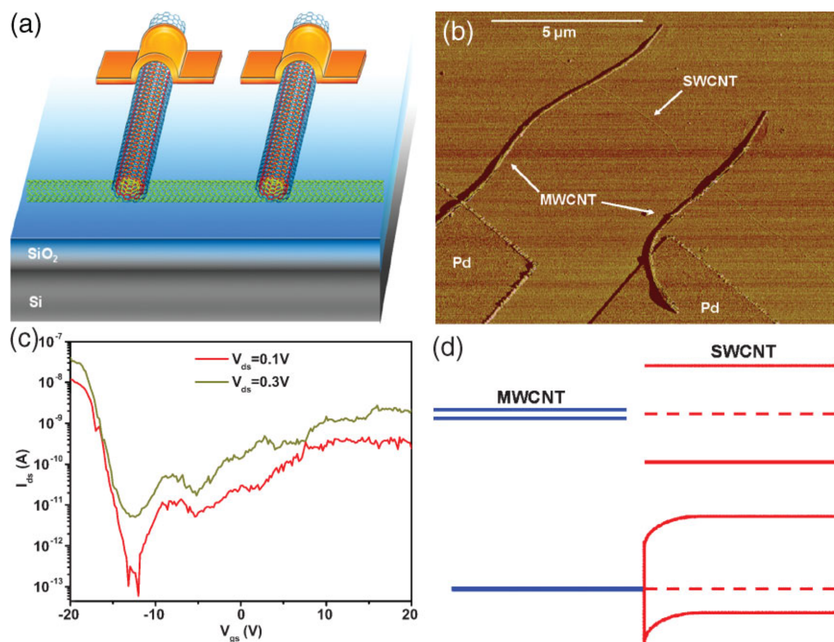

Figure 1. a) Schematic of a back-gated SWCNT FET that is locally interconnected by two MWCNTs and b) the corresponding AFM image of a real device. The diameter of the SWCNT is 1.5 nm and the channel length is 5.4 μm. c) Field-transfer characteristics of the device shown in b). I_{ds}: drain–source current; V_{gs}: gate–source voltage. d) Energy-band diagrams of the MWCNT, SWCNT, and a lightly p-doped MCWNT/SWCNT contact.

Depicted in Figure 1a is a semiconducting SWCNT that is directly contacted by two MWCNTs; the MWCNTs are then connected (to an external measurement circuit) by metal electrodes. The atomic force microscopy (AFM) image in Figure 1b shows the top view of a real device. The device structure shown in Figure 1a is the simplest structure of a whole-carbon FET, where the semiconducting SWCNT together with the back gate below it serves as the switch, and the directly connected MWCNTs are used as local interconnects. The two metal electrodes (Pd) are used as higher-level interconnects that are connected to an external circuit for electrical and field-effect measurements. Although each shell of a MWCNT can be either metallic or semiconducting, the electrical property of a large-diameter MWCNT does not depend sensitively on the details of the MWCNT structure, that is, whether a particular shell is metallic or semiconducting. This is because the band-gap of a semiconducting CNT is inversely proportional to its diameter[24] and, as a result, a semiconducting CNT can be regarded as metallic at room temperature once its diameter is above 30 nm, or its band-gap (26 meV) is less than the room-temperature thermal energy (26 meV). The MWCNT used in this work had an outer diameter of approximately 50–80 nm, and inner diameter of 10–20 nm (see Supporting Information, Fig. S1). It therefore makes no difference whether the outermost shell of the MWCNT (being contacted directly to the SWCNT) is metallic or semiconducting. The measured transfer characteristics of the whole CNT device are shown in Figure 1c, exhibiting an obvious field effect with an on/off current ratio of more than 10^5 at a drain–source voltage, V_{ds}, of 0.1 V. Figure 1c shows a basically ambipolar behavior, and this may be understood by the energy-band diagram shown in Figure 1d. The band-gap of a large-diameter MWCNT at room temperature is very small compared with that of a small SWCNT with a diameter of approximately 1.5 nm. The intrinsic MWCNT can then be effectively regarded as a metal with a work function (4.8 eV) that is almost the same as that of an intrinsic SWCNT. This is because both CNTs are formed by rolled graphene sheets. When a MWCNT is directly contacted to a semiconducting SWCNT, a Schottky barrier (SB) that has almost the same height with respect to both the valence and conduction bands of the SWCNT will be formed at the boundary[25] (upper panel of Fig. 1d). In principle, this SB, which is symmetric with respect to the conduction and valance bands, then results in symmetric ambipolar field-effect characteristics. However, the negative charges on the SiO_2 substrate dope the SWCNT to render it p-type;[26] the Fermi level of the system therefore shifts downward a little (lower panel of Fig. 1d), resulting in a more p- than n-type behavior. This doping effect is not strong, and the on-state current in the p-region is only about ten times larger than that in the n-region, as shown in Figure 1c. It should be noted that substrate doping may not be the only reason for the nonsymmetric ambiploar behavior, but it is now well-established that FETs fabricated on SiO_2 using as-grown SWCNTs exhibit p-type field-effect characteristics.

While the ambipolar-type field-effect characteristics of the whole CNT device shown in Figure 1 may be utilized in optoelectronics applications,[3] this behavior is not suitable for CMOS applications, where both n- and p-type unipolar FETs are required. In order to solve this problem, moderate amounts of Pd (or Sc) were deposited on the MWCNT/SWCNT contact, to convert it from an SB-type to a p-type (using Pd) or n-type (using Sc) contact (to the SWCNT), resulting in barrier-free injection of holes or electrons into the SWCNT.[5,27] Figure 2 shows an example in which Pd was used to obtain a p-type unipolar device. A schematic of the device is shown in Figure 2a, and an SEM image of a real device is shown in Figure 2b. Although in this device a large area at the MWCNT/SWCNT contact is covered by Pd (A or B in Fig. 2b), such a large area is not necessary to modify the contact from SB type to n- or p-type. The reason for using the configuration shown in Figure 2b is that it allowed the properties of each component of the device to be measured separately. The output and transfer characteristics shown in Figure 2c and d were measured directly using the A and B electrodes as source (S) and drain (D), respectively, via an A–SWCNT–B configuration. The linear on-state current–voltage I_{ds}–V_{ds} characteristics (Fig. 2c) at low bias suggest that the contacts between the metal (Pd) S and D electrodes and SWCNT are Ohmic, and the transfer characteristics (Fig. 2d) show that the device is a reasonably good unipolar p-type FET. The two-terminal on-state resistance of the SWCNT was determined from Figure 2d to be less than 1 MΩ at 0.1 V, which is reasonable for such a long-channel device (ca. 3.8 μm).

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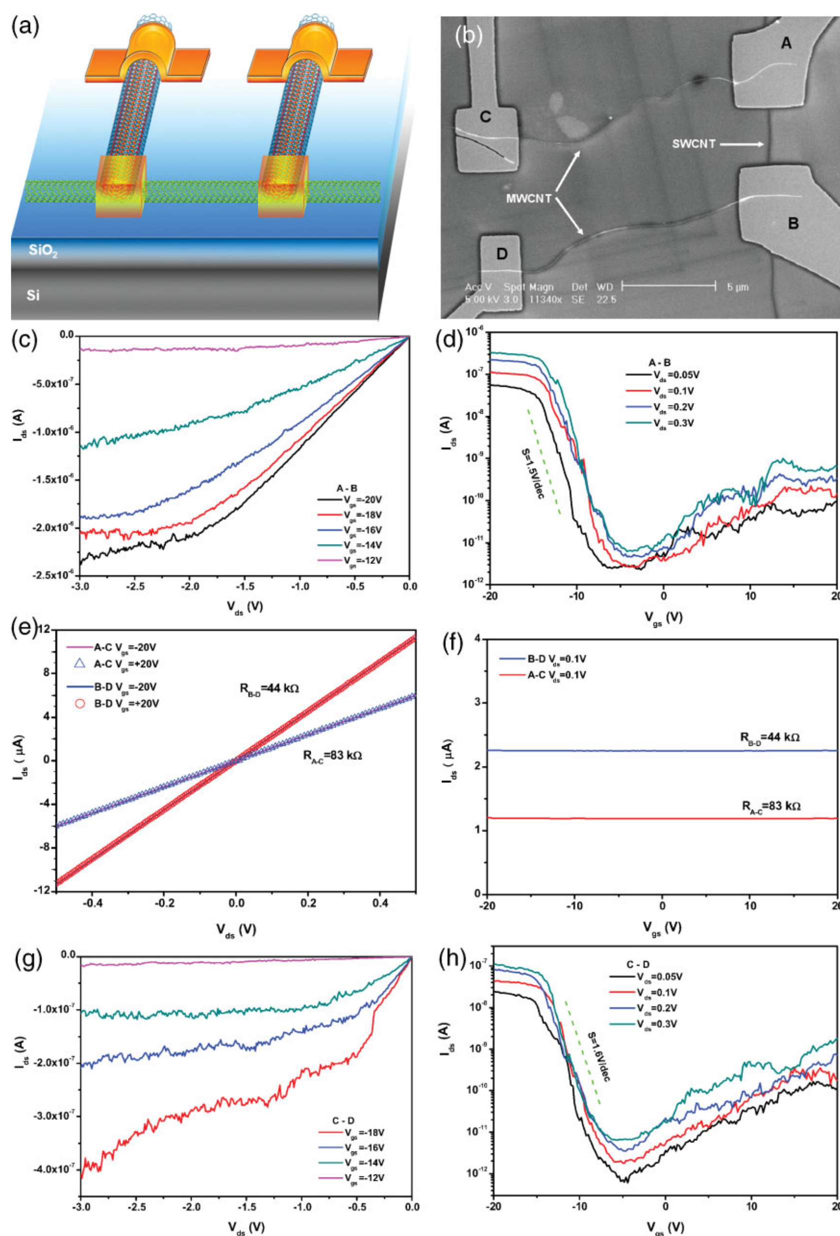

Figure 2. p-Type MWCNT-contacted SWCNT FET. a) Schematic and b) corresponding SEM image, showing the SWCNT being locally interconnected by two MWCNTs. When back-gated by the doped Si substrate beneath the SiO_2 layer, the structure behaves as a MWCNT-contacted SWCNT FET. c) I_{ds}–V_{ds} and d) transfer characteristics of the device shown in b) when measured using electrodes A and B as source and drain, respectively. Shown in e–h) are similar I_{ds}–V_{ds} curves and transfer characteristics of the two MWCNTs measured using e) A–C, f) B–D, and g,h) the MWCNT-interconnected SWCNT FET C–MWCNT–SWCNT–MWCNT–D. The diameter of the SWCNT is 1.5 nm and the channel length is 3.8 µm. The diameters of the two MWCNTs are 52 (A–C) and 64 nm (B–D).

The electrical properties of the two MWCNTs were measured using metal electrodes A and C or B and D. The I_{ds}–V_{ds} and transfer characteristics shown in Figure 2e and f suggest that the two MWCNTs are both good metals, showing perfect linear I_{ds}–V_{ds} characteristics and hardly any modulation of I_{ds} by the gate voltage, V_g. This verifies clearly that the MWCNTs are effectively metallic, and can be used for interconnects. The two-terminal resistance of the MWCNT between A and C is about 83 kΩ, which is higher than that between B and D (about 44 kΩ). This may be attributed to the fact that the MWCNT between A and C has a smaller diameter and is longer than that between B and D. The field-effect characteristics of the SWCNT with these two MWCNTs as local interconnects were measured by electrodes C and D (C–MWCNT–SWCNT–MWCNT–D), and the results are shown in Figure 2g and h. Both the I_{ds}–V_{ds} and transfer characteristics look similar to those measured using electrodes A and B (see Fig. 2c and d), but with reduced current. The reduced current is largely caused by the additional contact resistance between external (Pd) electrodes and MWCNTs and, in principle, this resistance may be reduced if the many shells of the MWCNT can all be utilized.[28] The characteristics in Figure 2d and h have very similar sub-threshold swings and almost the same on and off voltages. These results amply demonstrate that MWCNTs can be used as local interconnects for contacting SWCNT FETs while not compromising the main features of the device. The ambipolar-to-unipolar conversion can also be determined by comparing Figure 1c with Figure 2f; the on-state current ratio between the p- and n-region is improved from ∼10 to ∼100. The unipolarity can be further increased by using SWCNTs of smaller diameter. The measurements could also have been carried out between B and C or A and D, where only one MWCNT was used as the interconnect; the results are provided in the Supporting Information (Fig. S2). Similarly, MWCNT-contacted n-type SWCNT FETs may be obtained by depositing Sc on the MWCNT/SWCNT contact area.[5] The transfer characteristics of such an SWCNT FET are given in Figure 3, showing clearly that the FET is n-type.

Since both the p- and n-type MWCNT-contacted SWCNT FETs can be fabricated on the same SWCNT, a CNT-based CMOS inverter can then be constructed by combining one n-type and one p-type FET; the result of such a simple CMOS circuit fabricated on a single SWCNT is shown in Figure 4. The gain of the inverter is about three, which is indeed good for such a back-gated geometry with 500 nm thick SiO_2. Furthermore, the output high level (V_{out}) of the inverter is almost equal to the supplied voltage (V_{dd} = 3V), and the output low level is almost 0 V, affording almost perfect higher and lower digital levels. When the input was set to 0 V (3 V), an output 3 V (0 V) was obtained, showing perfect logical inversion. These results indicate that the CNT-based inverter works well, which will be beneficial for

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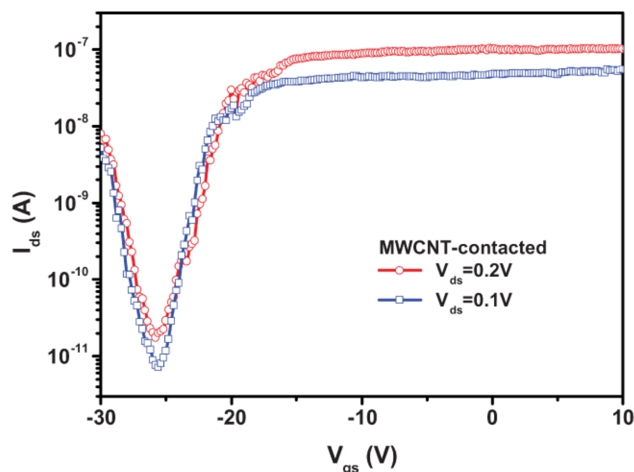

Figure 3. Measured field-transfer characteristics from an n-type MWCNT-contacted SWCNT FET. The diameter of the SWCNT is 1.6 nm and the channel length is 2.8 μm.

logical-circuit design. In principle, more complicated logical circuits, such as ring oscillators,[29] can be fabricated using the same procedure.

It is clear that the MWCNT-contacted SWCNT FET works well. However, there are some issues that need further clarification. In this work, Pd or Sc was deposited onto the junction between the MWCNT and SWCNT to define a p-type or n-type contact (or FET). It should be noted, however, that this is still a doping-free technology, in the sense that the electrical properties of the MWCNT and the SWCNT are not significantly modified. Instead, Pd (Sc) helps to align the Fermi level of the MWCNT to the valence (conduction) band of the SWCNT, thus helping to realize a p-type (n-type) SWCNT FET. There are two reasons for using MWCNTs rather than metallic SWCNTs as the local interconnects. The first reason is that all large-diameter MWCNTs can be

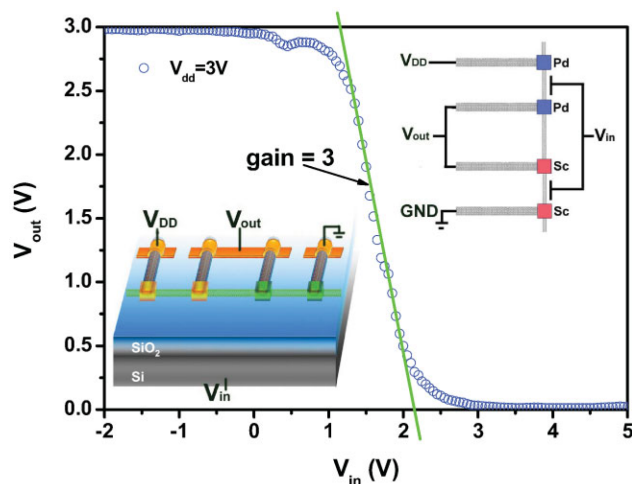

Figure 4. Input and output characteristics measured from a MWCNT-interconnected SWCNT inverter fabricated on one SWCNT. The diameter of the SWCNT is about 1.5 nm and the nominal channel length of the p- and n-FETs is 4 μm. Insets: schematics of the inverter.

used effectively as metal leads at room temperature regardless of the detailed structure of their individual shells. On the other hand, if metallic SWCNTs are to be used, they must first be separated from the semiconducting ones, which still remains a challenge. The second reason is that it is easy to obtain multichannel ballistic transport in MWCNTs, which can reduce the contact resistance of the MWCNT interconnects to a surprisingly low value.[28] The problem with the MWCNT interconnects is that usually only one or several outermost shells of the MWCNT contribute to the electrical conduction,[30,31] adding quantum resistance to the contact resistance and reducing the total current (see Fig. 2). It is therefore highly desirable to be able to utilize more shells of the MWCNT in real device configurations. Large hysteresis is usually observed in the transfer characteristics of back-gate geometry devices without passivation, and such hysteresis was also observed in the devices investigated here. This is one of the main reasons why the performance of the present devices is not as good as that of previously reported devices.[18–23] The hysteresis also impacts on the inverter (see Supporting Information, Fig. S3). On reversing the sweeping range and direction of the input voltage, the obtained gain usually varies in the range 1–4 (3 is a typical value, as shown in Fig. 4). By integrating the device with a top-gate and a high-*k* gate dielectric, for example HfO_2, the performance of the device will be greatly improved. The diameter of the MWCNTs used here was ∼50–80 nm, which can be scaled down to at least 30 nm, where the band-gap (26 meV) becomes comparable to the room-temperature thermal energy. Below 30 nm, metallic SWCNTs or few-shell CNTs should be used as interconnects.

In this work, a nanomanipulator was used to place the MWCNTs on to the SWCNTs. While it is arguable that this fabrication process is complicated and that the performance of the devices is not yet comparable to the best-performing top-gate devices, this work demonstrates the feasibility of integrating MWCNTs as local interconnects in SWCNT FETs. Combining the results from previous studies, where MWCNTs have been used as intermediate and global interconnects, circuits made entirely from CNTs may in principle be fabricated. In addition, the fabrication procedure used in this work may be further simplified using recently developed methods[32,33] to assemble MWCNTs onto SWCNTs on a large scale. These methods include the dielectrophoresis and Langmuir–Blodgett film assembly methods. The performance of our devices is not as good as that of some other reported devices,[18–23] but this is mainly because in this work a back-gate geometry was employed, and the gate oxide (SiO_2) was rather thick (500 nm). In principle, both can be avoided by integrating the device with a top-gate and a high-*k* gate dielectric, such as HfO_2. It has been demonstrated that CNT-interconnected silicon integrated circuits can be operated above 1 GHz.[17] The inherent high-frequency performance of these MWCNT-interconnected SWCNT FETs deserves further investigation, which is our next goal. People have dreamed of whole-carbon circuits by growing CNT networks.[34] However, this is only a distant dream, since growing such a network is still impossible. And even if such growth could be realized, defining p-type and n-type devices still remains a challenge. On the contrary, our strategy seems to be practical and we expect that it could provide an alternative for future integrated circuits.

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In summary, we have fabricated SWCNT FETs using MWCNTs as local interconnects, and have shown that the thus-fabricated device works well. When directly contacting the semiconducting SWCNT with two large-diameter MWCNTs, the resulting MWCNT-contacted SWCNT FET is basically a Schottky barrier FET, exhibiting an ambipolar field-transfer characteristic. The MWCNT-contacted SWCNT FET may be readily modified by depositing Pd (Sc) onto the MWCNT/SWCNT contact region to obtain a unipolar p-type (n-type) SWCNT FET and, by combining the thus-fabricated n-type and p-type SWCNT FETs, a high-performance CMOS inverter is obtained. Although in this work only MWCNTs were used as local interconnects, higher-level MWCNT interconnects have also been demonstrated previously by other groups. This work thus paves the way for whole-carbon integrated circuits.

Experimental

Both SWCNTs and MWCNTs used in this work were grown by chemical vapor deposition [35] on a heavily doped Si substrate that was covered by a 500 nm thick thermally grown SiO_2 layer. After identifying a semiconducting SWCNT, MWCNTs were positioned onto it using a nanomanipulator (Kleindiek) [36] in a scanning electron microscope (see Supporting Information, Fig. S4). Final electrodes for measurements were defined by electron-beam lithography, and then Pd or Sc was deposited by electron-beam evaporation followed by lift-off. The heavily doped Si was used in this work as the back gate, and all electrical measurements were carried out with a Keithley 4200 semiconductor characterization system at room temperature.

Acknowledgements

This work was supported by the Ministry of Science and Technology (Grant No. 2006CB932401, 2006CB932402, 2006AA03Z350), and National Science Foundation of China (Grant Nos. 60571002, 10434010, and 90606026). Supporting Information is available online from Wiley InterScience or from the author.

Received: September 17, 2008
Revised: December 2, 2008
Published online: February 19, 2009

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